Temperature Nonuniformity and Bias-Dependent Thermal Resistance in Multi-Finger MOS Transistors

Xi Wang*, Ali Shakouri**, Jacob Wysocki, Mike Wincn and Ken Petrotti
Electrical Engineering Department, University of California, Santa Cruz, CA, 95064
1156 High Street, Santa Cruz, CA, 95064
*wangxi@soe.ucsc.edu; **ali@soe.ucsc.edu

Abstract

In this paper, we study self-heating in a multi-finger MOSFET transistor. Different source-drain voltages are applied so that the transistor is in triode and saturation regimes. Thermoreflectance imaging technique was used to obtain high resolution thermal images of the transistor. This allowed us to obtain profiles with high spatial and temperature resolution. We verified that the actual size and shape of the heating source are modified as the biasing condition changes. Detailed comparison between the measurement results and analytical calculations proves that the thermal resistance of transistor is dependent on the biasing condition. It can change by a factor bigger than 5 for different drain-source voltages. Even in the saturation regime, the thermal resistance of the transistor can change by 50% as a function of bias.

1. Introduction

Thermal issues are one of the key factors limiting the performance and reliability of the state-of-the-art electronic, optoelectronic devices and integrated circuits. As switching speeds increase and devices are further miniaturized, localized heating problems are exasperated [1, 2]. Systematic characterizations of temperature distribution inside devices and interconnections are very important.

A field-effect-transistor (FET) is a three terminal device, where a non-uniform electrical potential distribution is naturally created. This electrical potential field together with the current flow along the channel generates a non-uniform temperature distribution (*hot-spot*), which is usually located towards the drain end for a typical MOSFET. The introduction of novel geometries and materials in modern transistors have made non-uniform self-heating effects even more pronounced.

Non-contact thermoreflectance imaging is capable to obtain thermal images with both high spatial resolution (sub-micron) and temperature resolution (sub-Kelvin) [3, 4]. It has recently been utilized to characterize heating effects in MOS transistors [5]. However, Mihai *et al*.'s work emphasized on demonstrating the applicability of the experimental system, but did not provide detailed discussions about the heating inside the transistor.

In this study, we have performed systematic thermal characterization and analyses of an n-type depletion mode multi-finger MOSFET. The following section describes the experimental setup used to obtain surface temperature distribution. Device layout is shown in section 3. Thermal images are presented at various biasing conditions in both triode and saturation regimes. In section 4, we discuss different results and introduce the bias-dependent thermal resistance of the transistor.

2. Experimental Setup

Thermoreflectance technique is based on the change of the sample surface reflection coefficient as a function of temperature. This small change in 10^{-4}~10^{-5} range per degree is typically detected using lock-in technique when the temperature of the device is cycled [3, 4]. Images are detected by either a PIN diode array camera or a high frame rate Intensified CCD (ICCD). The PIN array has a higher dynamic range and thermal resolution, while the ICCD yields superior spatial resolution. In this experiment, ICCD was used as we were interested in the high spatial resolution temperature distribution in the device in steady state.

Fig. 1 shows the thermoreflectance imaging setup. A beam of 455nm blue light emitted from a high power LED was focused onto the sample through a high magnification objective (80X). The reflected image was then projected onto the ICCD detector that is controlled by computer.

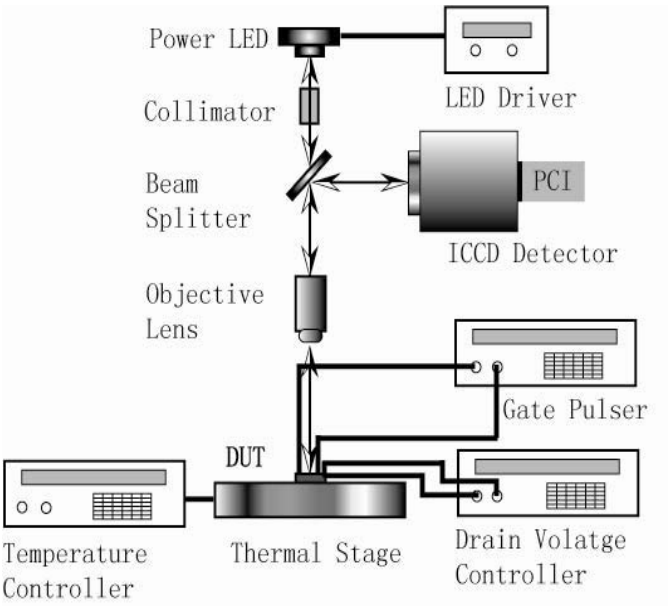

Figure 1: Schematic of the thermoreflectance imaging setup.

A thermal stage was place immediately underneath the sample to provide an efficient heat dissipation path. While taking the thermal image, pulsed voltage was applied to the gate terminal, and the drain-source voltage was hold at a constant level, so that the imaging system can capture the surface temperature changes when the MOS transistor is in "ON" state.

3. Device and Experimental Results

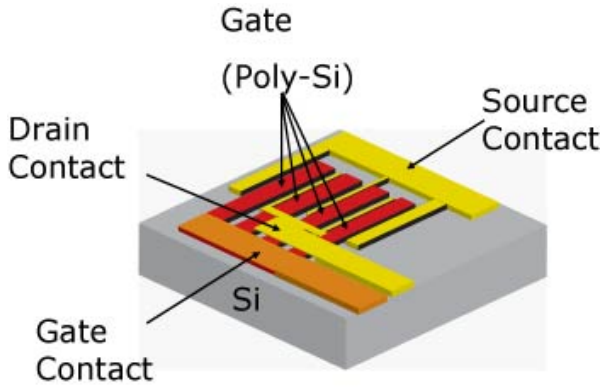

Figure 2: Schematic of the multi-finger MOSFET.

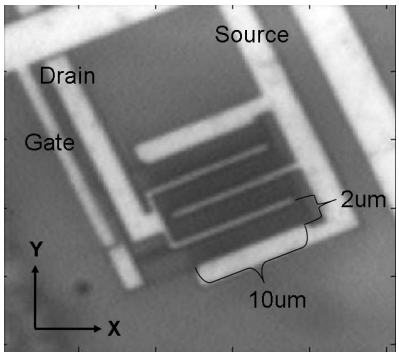

Figure 3: Geometry of the measured MOSFET device.

Shown in Fig. 2 and Fig. 3 are the schematics of the structure and geometry of the measured multi-finger MOSFET device. Multiple gates/channels are used to increase the operating current and we are interested to study temperature distribution in the device. Fig. 4 shows the surface temperature rise of the multi-finger MOSFET when different biasing conditions (V_{ds} =0-4 volt, V_{gate} = 2 volt) are applied.

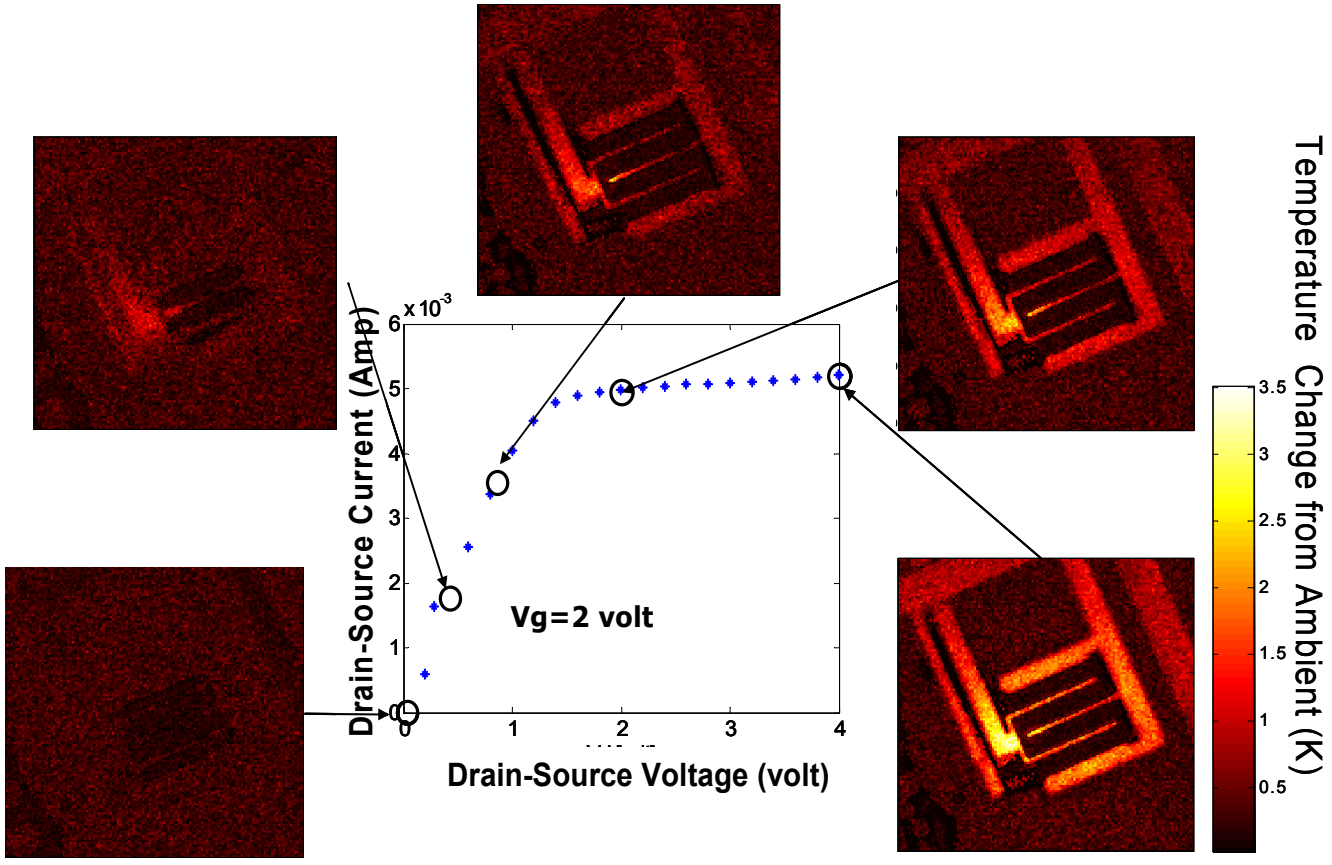

Figure 4: Thermoreflectance images of the multi-finger MOSFET under different biasing conditions. Temperature profile is calibrated on the metal layer.

4. Discussions

Typically, electro-thermal modeling is based on an assumption that the thermal resistance of the device is independent of the applied voltage. If this assumption is valid, the temperature rise at hot-spot should be linearly increases as the input power increases, as described in Equation 1. ΔQ represents the amount of power being dissipated (measured through the current-voltage characteristics), ΔT is the expected temperature change at hot-spot and R_{th} is the total thermal resistance in the heat flow path.

$$\Delta T_h = \frac{\Delta Q}{R_{th}}, \qquad <1>$$

However, plotting the hot-spot temperature rise and also power dissipation versus source-drain voltage, we noticed a discrepancy (see Fig. 5). Before the device reaches pinch-off, the hot-spot temperature increases in rather a parabolic trend than in a quadratic trend as the input power does. After pinch-off, although the trends of hot-spot temperature rise increment and input power increment are both quasi-linear, the slopes are very different. This violates the Fourier's law if assuming a constant thermal resistance in the heat flow path.

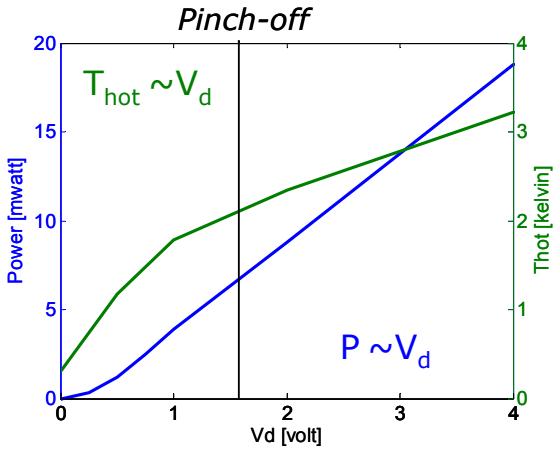

Figure 5: Hot-spot temperature and input power versus source-drain voltage.

We further analyzed the measured thermal images. Shown in Fig. 6 is a comparison between the input power and an integral of temperature within the hot-spot area. Hot-spot area is determined by setting a threshold temperature rise of 1.0 Kelvin. Similar trends for the power dissipation and for the temperature integral are found as a function of bias both before and after pinch off. This indicates that the discrepancy revealed in Fig. 5 is caused by the evolution of actual size/shape of the hot-spot when the drain-source voltage is changed. The small difference between slops could be due to the lack of temperature signal in the poly-gate area, where the thermoreflectance coefficient is small at the wavelength we used in this experiment.

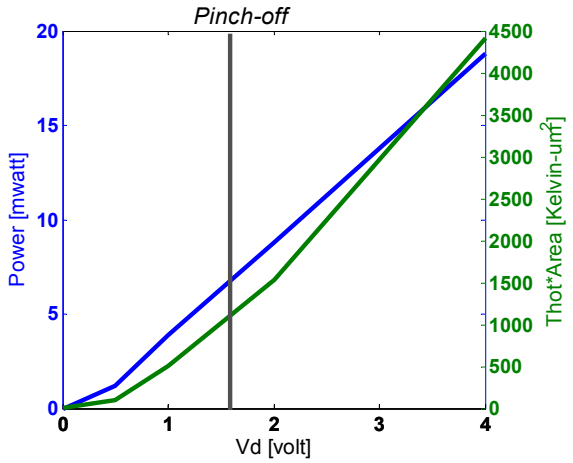

Figure 6: Input power and temperature integral (i.e. temperature rise times hot spot area (Kelvin-μm^2)) versus source-drain voltage.

To simulate the actual thermal resistance at different biasing condition, we utilized a spreading thermal resistance model [6]. We approximated that the heating source has a circular contour defined by a radius, r_h, This heat source is sitting on a silicon substrate with radius significantly larger than that of the hot-spot. A ceramic package is introduced as the boundary condition at the bottom surface of the silicon substrate. Equation 2 represents the spreading thermal resistance at the hot spot.

$$R_{th} = \frac{L_{sub}}{A_{sub}\kappa_{sub}} + \frac{1}{2a\kappa_{sub}\sqrt{\pi}}(1-\varepsilon)^{3/2}\Phi_C, \qquad <2>$$

Where,

$$\Phi_C = \frac{\tanh(\lambda_C\tau) + \frac{\lambda_C}{B}}{1 + \frac{\lambda_C}{B}\tanh(\lambda_C\tau)}, \qquad <3>$$

$$a = \sqrt{\frac{A_h}{\pi}},\ b = \sqrt{\frac{A_{sub}}{\pi}},\ \varepsilon = \frac{a}{b},\ \tau = \frac{L_{sub}}{b}, \qquad <4>$$

$$\lambda_C = \pi + \frac{1}{\varepsilon\sqrt{\pi}},\ B = \frac{hA_{sub}}{\pi\kappa_{sub}b}, \qquad <5>$$

A_h and A_{sub} are the areas of heat source and substrate surface. κ_{sub} is thermal conductivity of silicon substrate. a, b, ε, and λ_C are dimensionless coefficients. h is the heat transfer coefficient, which can be estimated as

$$h = \frac{1}{R_f A_{sub}} \qquad <6>$$

where R_f is the thermal resistance of the ceramic package.

Based on the geometry and material properties listed in table 1, we simulated the spreading thermal resistance at the hot-spot as a function of its radius.

Layer	Radius (μm)	Thicknes s (μm)	Thermal conductivity ($w/\mu m - K$)
Hot-spot	2~20	N/A	N/A
Silicon	1000	500	1.3e-4
Package	N/A	1000	17e-6

Table 1: Geometry and material properties.

Shown in Fig. 7 is a comparison between the simulated spreading thermal resistances and extracted thermal resistances from measurement results. The later was calculated using Equation 1. The radiuses of the experimentally observed hot-spots were determined by setting a temperature threshold of 1.0 Kelvin. A good fit between simulation and experiment was found.

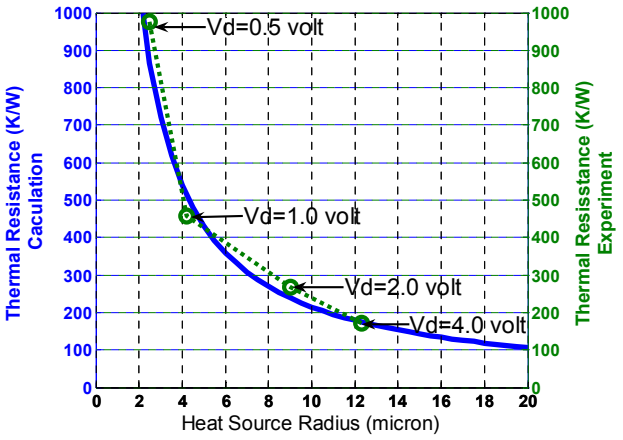

Figure 7: Theoretical and experimental device thermal resistance versus heat source radius assuming three-dimensional heat dissipation on silicon substrate.

5. Conclusions

In this paper we performed a systemic thermal characterization of a multi-finger MOSFET. We obtained high resolution thermal images using thermoreflectance technique. Taking advantages from the full-field imaging capability of thermoreflectance technique, we quantified the size/shape change of hot-spot at various biasing conditions. We also verified the dependency of transistor thermal resistance on biasing conditions through comparison between simulation and experiment.

Conventionally, in the electro-thermal modeling of high power transistors, the transistor thermal resistance is extracted at small biases and short pulses and it is assumed to be a constant depending only on the geometry of the transistor [7]. We anticipate that the bias-dependent transistor thermal resistance will play an important role in compact design of the chips and in high power circuits.

Acknowledgments

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