High-power-density spot cooling using bulk thermoelectrics

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We demonstrate a three-dimensional (3D) bulk silicon microcooler, which has the advantages of high cooling power densities and is less dependent on thermoelectric element's thickness as compared with the same device with one-dimensional (1D) geometry. We measured a maximum cooling of 1.2 °C for a 40×40 μm^2 area bulk silicon microcooler device, which is equivalent to an estimated cooling power density of 580 W/cm^2. In this unique geometry, both current and heat spreading in 3D allows the maximum cooling temperature to exceed the conventional 1D thermoelectric model's theoretical limit 0.5 ZT_c^2. © *2004 American Institute of Physics*.
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The conventional thermoelectric coolers (TEC) are analyzed with one-dimensional (1D) current continuity and heat conduction equations. Thus the performance of a single element TEC could be analyzed with the equation: $Q=\alpha IT_c-1/2I^2R-\Delta T/R_{th}$, where α is the Seebeck coefficient; I the current; T_c the cold side temperature; R the electrical resistance of the TEC element; and R_{th} thermal resistance of the TEC element.[1] From this equation, we can find the optimized current to achieve the maximum cooling (ΔT_{max}), which is 0.5 ZT_c^2. Z is called the figure of merit, which can be described by the equation $Z=\alpha^2/\rho\kappa$.[2] This ΔT_{max} is the theoretical limit that a 1D device can achieve based on the materials' properties, which are independent of the device's area and leg length. Similarly we can find out the maximum cooling power (Q_c) that can be achieved when ΔT is close to zero with the equation $Q_c=1/2\alpha^2T_cA/\rho L$. Because the cooling power is inversely proportional to the TEC leg length, the TEC geometry needs to be optimized to improve its cooling power density (CPD).[3–6]

In this letter we describe the fabrication of a bulk silicon microcooler with three-dimensional (3D) geometry. This geometry is similar to the previously demonstrated SiGe/Si[7] and SiGeC/Si[8] superlattice coolers, for which we considered the combined effects of 3D current and heat spreading through the superlattice structure. In this analysis we only consider bulk materials with 3D geometry. Figure 1 is a scanning electron microscope (SEM) image of an array of 3D silicon microcoolers with various device sizes. The bulk silicon is p-type boron doped at a doping concentration of 10^{19} cm^{-3}; its resistivity ranges from 0.001 to 0.006 Ω cm. The device was fabricated with standard microfabrication techniques: dry etch, lithography, metal evaporation, etc …. The mesa was etched down to ~0.5 μm to form the device area. A Pt/Al/Pt/Au layer with a thickness of 0.1/1.0/0.1/1.5 μm was deposited as a metal contact. The probe contact area is extended to the side to avoid Joule heating of the probe, which can suppress cooling on top of the device area. A thin SiN_x layer underneath the probe contact area guides the current going through the probe, while preventing any current from leaking into the substrate before it reaches the device region. The injected current goes through the mesa and then spreads radically into the substrate along with the heat.

In this 3D design, the previous 1D theory is not appropriate. To evaluate the device's performance and analyze its limitations, we developed a 3D electrothermal model using ANSYS™ software.[9] In our model, bulk Joule heating and heat conduction are automatically calculated by solving current continuity and heat conduction equations. Thermoelectric cooling/heating is added as an interface effect whose value could be determined by $\Delta Q=(S_{metal}-S_{Si})TI$. To verify the model, the cooling below the ambient, $\Delta T=T_{ambient}-T_c$, was also experimentally measured with two Omega™ Type E thermocouples, each with a 50-μm-diam tip; one thermocouple on top of the device and the other one far away on the substrate. We estimated the range of the temperature resolution for this setup to be 0.05–0.1 °C. The sample was placed on a temperature controlled stage to keep the substrate temperature equal to the ambient temperature. A stable current was supplied to the refrigerator, stepping from 0 to 500 mA with a step size of 25 mA. The temperature difference was recorded at every step. We plotted the cooling versus supplied current from experimental measured data (cross, triangle, circle and square) with simulated cooling curves for various device sizes in Fig. 2. The simulated cooling curves

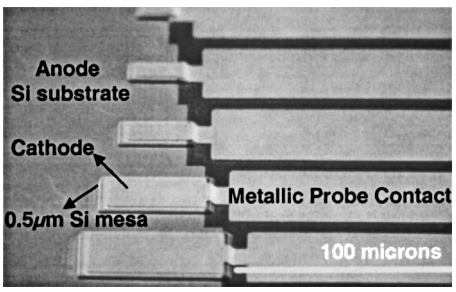

FIG. 1. A scanning electron microscope (SEM) picture of silicon microcooler array.

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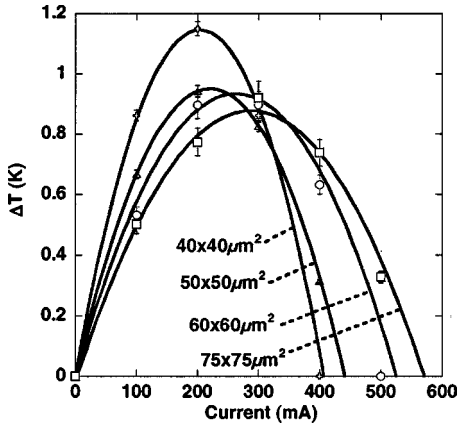

FIG. 2. Si microcooler, ΔT, vs supplied current for all device sizes. Points ($\diamond$, $\triangle$, °, $\square$) are experimental data for various device sizes, solid curves are simulated results.

fit well with the experimental data points for all device sizes with the standard deviation ~0.1.

With the 3D electrothermal model, the cooling power densities of the devices can also be estimated. We could apply the heat flux on top of the microcooler, increasing the amount of heat flux until it reaches the point where there is no refrigeration, $\Delta T=0$. At this point, the amount of heat flux on top of the microcooler is what we define the cooling power of the device to be, as indicated in Fig. 3. The estimated cooling power density (CPD) of a 40×40 μm^2 device is 580 W/cm^2 and a 75×75 μm^2 device 250 W/cm^2.

In our experimental devices there are many nonideal effects including Joule heating from contact probe and metal-semiconductor contact resistance. These nonideal factors influence our intuition on the materials' intrinsic properties. Thus we simplified the model in ANSYS™ by considering an ideal bulk silicon block with a surface area 300×300 μm^2. For a 1D device the whole top surface was used as contact surface; for a 3D device the device contact area was anywhere from 5×5, 50×50, 100×100, and 150×150 μm^2, as illustrated in Fig. 4. The Peltier cooling was added as the surface effect at the contact area. In the 1D device the maximum cooling obtained from our model, $\Delta T_{max}=1.26$ °C, agreed with the theoretical predictions obtained by the equation, $\Delta T_{max}=0.5\ ZT_c^2$ (the empirical Z value, 3.3×10^{-5} K^{-1}, was used). In the 1D model, when the thickness of the silicon ranges from 10 to 700 μm the ΔT_{max} remains constant, but

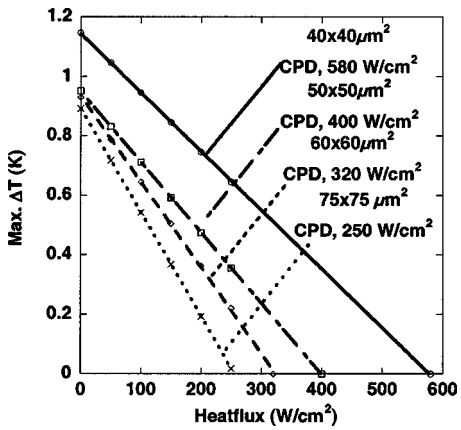

FIG. 3. ΔT_{max} vs applied heat load flux with estimated cooling power density (CPD) (simulation).

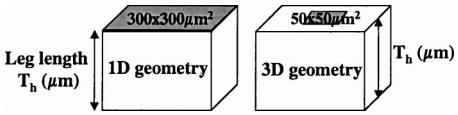

FIG. 4. Schematic of an ideal 1D and 3D bulk TEC.

the optimized current I_{opt} changes inversely with the thickness. However, the 3D device yields a different scenario: the maximum cooling varies from 1.6 to 2.8 °C. The best cooling, 2.8 °C, only occurs at an optimized thickness, which varies with device areas. For example, the optimized thickness for the 100×100 μm^2 device is 50 μm. Only when the device size is extremely small, like 5×5 μm^2, is the maximum cooling, $\Delta T_{max}=2.8$ °C, independent of the device thickness. According to the model, the 3D geometry more than doubles the cooling of a 1D device. This is mainly due to the current and heat spreading, which effectively reduces the overall Joule heating flowing back to the cold junction.

Using the 3D device geometry could also alleviate problems that conventional TECs always have: low CPDs and CPDs with heavy dependence on leg lengths.[3,5,10] Figure 5 illustrates the comparison of the CPDs versus substrate's thickness (T_h) for a 1D device, and a 3D device with 50×50 μm^2 contact area. We can see that a 1D device's CPD is inversely proportional to the substrate's thickness, however 3D devices' CPDs are inversely proportional to the root mean square of the substrate's thickness, which could be represented by the equation $CPD=m_1+m_2/\sqrt{T_h}$ (m_1, m_2 are constants) for all devices ranging from 50×50 μm^2 to 150×150 μm^2. Only when the device contact area is extremely small, like 5×5 μm^2, does this relationship break down. As shown in Fig. 5, the CPD of such a small device is almost a constant, independent of substrate thickness. Thus we could conclude the 3D geometry facilitates a CPD that is 2–24 times better than the 1D device as the substrate thickness (T_h) ranges from 10 to 700 μm. In Fig. 6 we also plot the CPD versus device area for a 3D bulk Si device with different substrate thicknesses. It is interesting to find out that the CPD becomes saturated when the device area is larger than 100×100 μm^2. For example, contact areas of 100×100 and 150×150 μm^2 for a 500-μm-thick bulk silicon substrate device would have the same amount of CPD ~300 W/cm^2.

It is also expected that the 3D bulk TE device will have a much higher coefficient of performance (COP) than the 1D

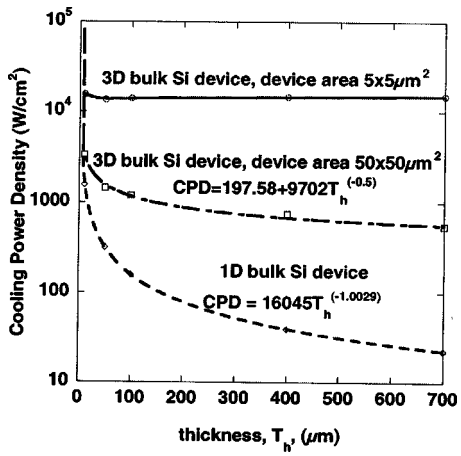

FIG. 5. Comparison of CPD vs substrate's thickness (T_h) between 1D and 3D bulk TEC.

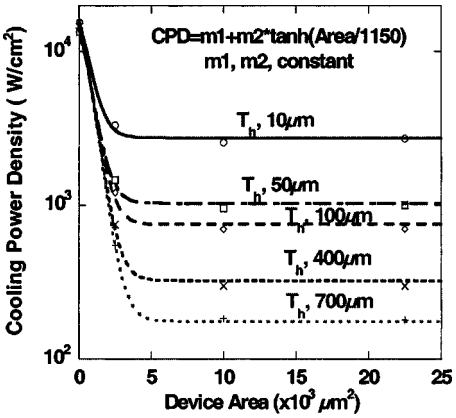

FIG. 6. Three-dimensional bulk Si device CPDs vs device area with different substrate's thickness, T_h, 10–700 μm.

device. Consider a 500-μm-thick bulk Si device that cools 1.26°C; a 1D geometry has a COP of 0.4, while the 3D geometry has 2.0, which is five times better.

In summary, when the materials' parameters are the same, the 3D bulk TE devices can exceed a 1D device's cooling capabilities by more than doubling the maximum cooling, $\Delta T_{\max}$, and increasing the cooling power densities 2–24 times. Experimentally, the bulk silicon microcooler (500 μm thick) achieved a maximum cooling of 1.2 °C or equivalently an estimated CPD of 580 W/cm^2. Based on these improvements, a 3D bulk microcooler is an attractive spot cooling solution for integrated circuits using substrate's thermoelectric properties.

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