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# FAST THERMAL ANALYSIS OF VERTICALLY INTEGRATED CIRCUITS (3-D ICS) USING POWER BLURRING METHOD

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## ABSTRACT

CMOS VLSI technology has been facing various technical challenges as the feature sizes scales down. To overcome the challenges imposed by the shrink of the conventional on-chip interconnect system in IC chips, alternative interconnect technologies are being developed: one of them is three dimensional chips (3D ICs). Even though 3D IC technology is a promising solution for interconnect bottlenecks, thermal issues can be exacerbated. Thermal-aware design and optimization will be more critical in 3D IC technology than conventional planar IC technology, and hence accurate temperature profiles of each active layer will become very important. In 3D ICs, temperature profile of one layer depends not only on its own power dissipation but also on the heat transferred from other layers. Thus, thermal considerations for 3D ICs need to be done in a holistic manner even if each layer can be designed and fabricated individually. Conventional grid-based temperature computation methods are accurate but are computationally expensive, especially for 3D ICs. To increase computational efficiency, we developed a matrix convolution technique, called Power Blurring (PB) for 3D ICs. The temperature resulting from any arbitrary power dissipation in each layer of the 3D chip can be computed quickly. The PB method has been validated against commercial FEA software, ANSYS. Our method yields good results with maximum error less than 2% for various case studies and reduces the computation time by a factor of ~ 60. The additional advantage is the possibility to evaluate different power dissipation profiles without the need to re-mesh the whole 3D chip structure.

## INTRODUCTION

The evolution of CMOS VLSI technology has been driven by two main motives: to increase functionality and functional density. The latter has been accomplished by aggressively scaling down the technology, along with increasing the number of metal layers [1]. According to the International Technology Roadmap for Semiconductors (ITRS) [2], interconnect has evolved from a single layer wiring to eleven layers over the past four decades, and the number of wiring layers is projected to increase further. Figure 1 shows a schematic cross-section of a multilevel interconnect scheme.

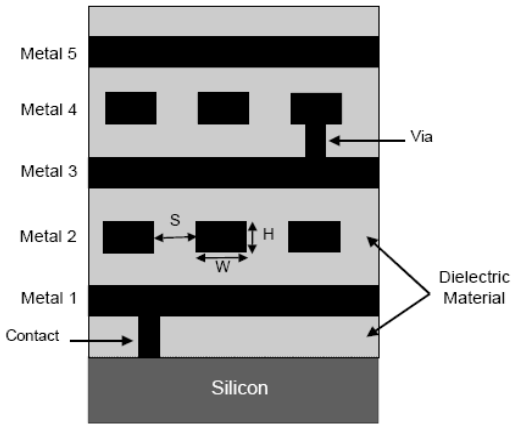



**FIGURE 1. A Schematic cross section of a multi-level interconnect scheme employed in present VLSI circuits (from [3]).**

The impact of on-chip interconnects on performance, reliability, and power consumption of VLSI ICs has increased dramatically as the technology continues to scale down into deep nanometer scale regime. Unlike devices, on-chip interconnects are adversely affected by technology scaling due to reduced metal pitch and increased number of metallization levels. These interconnects not only subject to thermal effects resulting from the power dissipation in devices but also cause thermal effects themselves such as self-heating (or Joule heating) [4, 5]. Additionally, low dielectric constant (low-k) materials are being introduced to reduce interconnect capacitance for enhancement of chip performance, which can

exacerbate thermal effects due to their poor thermal properties [3].

3D ICs has been proposed as an alternative interconnect technology to overcome the challenges imposed by the scaling of the conventional interconnect system. A 3D IC is formed by stacking two or more layers of active devices. Figure 2 illustrates the concept of 3D ICs, bonding approaches, and its package structure.

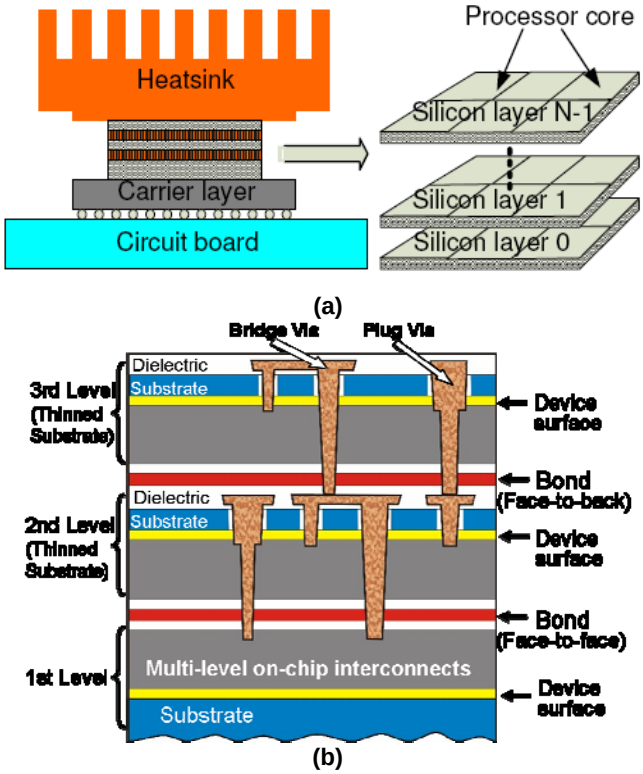



**FIGURE 2. (a) 3D Multiprocessor SoC (MPSoC) chip and package structure (from [6]) (b) 3D integration concept using wafer-bonding and bonding approaches of "face-to-face" and "face-to-back"(from [7]).**

3D integration scheme can significantly improve deep-submicrometer interconnect performance by reducing the number and the average length of global interconnects [8]. However, thermal issues can be aggravated because multiple active layers which dissipate power are stacked together with bonding materials of relatively low thermal conductivity. Non-uniform high temperatures have significant impact on chip performance and reliability, which will get worse in 3D IC technology. Thus thermal-aware design will be an essential aspect of 3D IC design and accurate temperature profiles of each active layer will be of great use. In 3D ICs, temperature profile of one layer depends not only on its own power dissipation but also on the heat transferred from other layers. Thus, thermal considerations for 3D ICs need to be done in a holistic manner even if each layer can be designed and fabricated separately [9].

Thermal analysis has been conventionally performed based on grid-based methods such as Finite Element Method (FEM) or Finite Difference Method (FDM). These methods are accurate but computationally expensive, especially for 3D ICs. To increase computational efficiency, we developed a matrix convolution technique, called Power Blurring (PB), for planar 2D ICs in the past [you should also include our first paper on power blurring in Therminic 2006, 10]. We extended our 2D IC PB method to accommodate 3D chip thermal analysis. In this paper, the PB method for 3D ICs will be discussed in detail, and case study results will be presented.

## NOMENCLATURE

| | |
|---|---|
| $k$ | Thermal conductivity [W/m·K] |
| $\rho$ | Density [kg/m$^3$] |
| $c_p$ | Specific heat [J/kg·K] |
| $q^*$ | Heat generation per volume [W/m$^3$] |
| $T$ | Temperature [K or C°] |

## FULL CHIP PACKAGE THERMAL MODEL

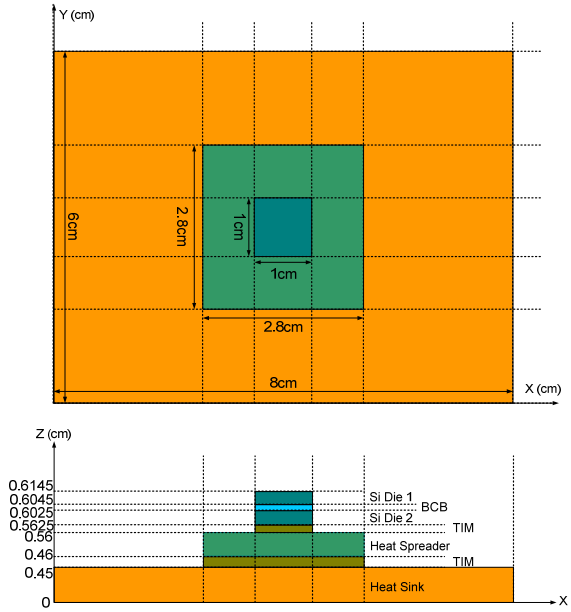



**FIGURE 3. Schematic of a packaged 3D IC chip, where the heat spreader, the heat sink and the thermal interface material (TIM) are included.**

Figure 3 shows our full chip package thermal model and material parameters and dimensions are summarized in Table 1. The configuration consists of two Si ICs with surface areas of 1cm×1cm and a Cu heat sink with a heat spreading layer. Thermal interface material (TIM) reduces the effect of surface roughness on the contact area and hence improves heat conduction at the interface. Assuming flip chip package, most of the heat is considered to flow through the bottom surface of

the heat sink, and other minor heat transfer paths are neglected; heat transfer coefficient of 0.15W/cm$^2$-K is employed for the bottom surface of the heat sink and adiabatic boundary condition is imposed on other surfaces. The Si ICs are orthogonally meshed with an element size of 0.025cm×0.025cm. 3D IC technology is an emerging technology and bonding process technologies are still being developed. In this study, we assumed bonding approach of adhesive polymer BCB (Benzocyclobutene) and "face-to-back" bonding [11, 12]

**TABLE 1. Material properties and dimensions of the package model.**

| | Area (mm$^2$) | Thickness (mm) | Thermal Conductivity (W/m-K) | Density (kg/m$^3$) | Specific Heat (J/kg-K) |
|---|---|---|---|---|---|
| Si Die 1 | 10×10 | 0.2 | 117.5 | 2330 | 700 |
| BCB | 10×10 | 0.02 | 0.2 | 1051 | 2187 |
| Si Die 2 | 10×10 | 0.5 | 117.5 | 2330 | 700 |
| TIM1 | 10×10 | 0.025 | 5.91 | 1930 | 15 |
| Heat Spreader | 28×28 | 1 | 395 | 8933 | 397 |
| TIM2 | 28×28 | 0.1 | 3.5 | 1100 | 1050 |
| Heat Sink | 60×80 | 4.5 | 395 | 8933 | 397 |

## POWER BLURRING FOR 3D IC

Governing equation for heat conduction is given by [13]

$$k\frac{\partial^2 T(x,y,z,t)}{\partial x^2}+k\frac{\partial^2 T(x,y,z,t)}{\partial y^2}+k\frac{\partial^2 T(x,y,z,t)}{\partial z^2}+q^* = \rho c_p \frac{\partial T(x,y,z,t)}{\partial t} \quad (1)$$

To obtain temperature distributions in a solid, Equation (1) needs to be solved with given boundary conditions. In thermal analysis of ICs, it has been handled by grid-based method such as FDM and FEM, or Green's function-based method.

With the Green's function method [14], a solution to the partial differential equation is obtained using a unit source (impulse) as the driving function, and then the solution to the actual driving function is written as a superposition of the impulse response with the unit source at different locations. The PB method is fundamentally similar to the Green's function method in that the PB method renders thermal profiles of a system based on the thermal impulse response of the system using superposition principle. The thermal impulse response of a system, which is named thermal mask, serves as the building block of final thermal profiles.

The thermal impulse response can be obtained by using a Finite Element Analysis (FEA) tool such as ANSYS [15] or by thermal imaging characterization. To generate a thermal mask, a point heat source (an approximate unit source) is applied to the center of the IC chip. Subsequently, the surface thermal profile obtained with the point heat source is normalized with respect to the amount of applied power. Then the thermal mask has the unit of thermal resistance (°C/W). Therefore, when the thermal mask is convolved with a given power map, it can generate a thermal profile corresponding to the power map. The basic concept of the Power Blurring method is illustrated in Fig. 4.

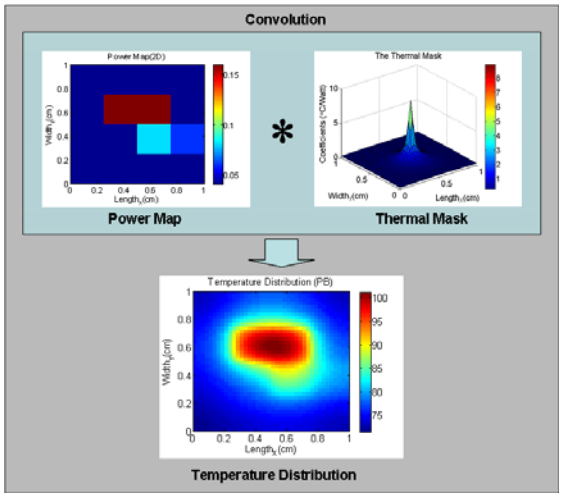



**FIGURE 4. Schematic illustration of the Power Blurring method.**

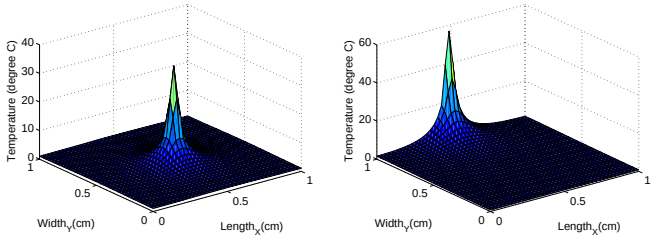



**FIGURE 5. Temperature profiles on the surface of an IC chip with a point heat source at different locations: (a) at the center; (b) at the edge.**

The shape of the impulse response depends on the location where the point heat source is applied. For example, a point heat source at the center and that at the edge of the IC surface produce different peak temperatures and different temperature profiles as shown in Fig. 5. Adiabatic boundary condition imposed on the side walls of Si die causes the edge effect. This is due to the finite size of an IC chip; hence, a point heat source applied to the edge is affected by the boundary condition more prominently. To be able to use a single thermal mask for the convolution, the thermal mask needs to be such that it is common to all the locations of the die. Thus, the most adequate location where the thermal mask can be obtained is the center of the chip in spite of the edge effect because, luckily, it can be taken care of by Method of Images [10]. Another correction is due to our realistic package model. 3D heat flow in the heat spreader and heat sink requires additional consideration of heat spreading. Heat spreading is incorporated by intrinsic error

compensation at every point of convolution. The intrinsic error is defined as the temperature deviation along the perimeter of the die for uniform power distribution due to heat spreading. This correction uses an extra ANSYS simulation of the temperature profile resulting from uniform heat dissipation in the chip [16]. An example of the intrinsic error profile is shown in Fig. 6.

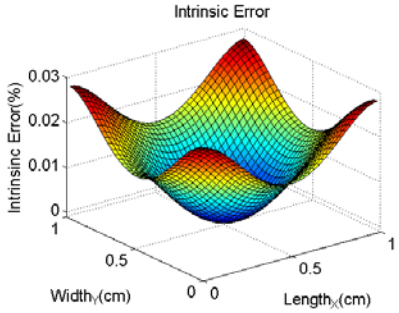
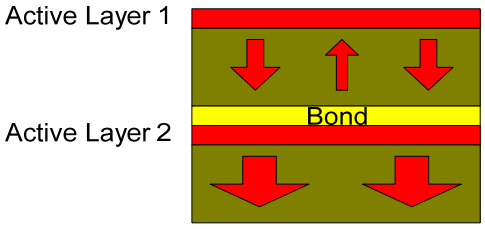



**FIGURE6. An example of intrinsic error profile: intrinsic error resulted from the uniform power distribution at the first layer.**

The original PB method for 2D ICs requires only one thermal mask whereas 3D IC PB method requires multiple thermal masks. This is due to the fact that thermal profile of an active layer is determined by not only its own power consumption but also heat transferred from other active layers as shown in Fig. 7. The temperature profile of each active layer is determined by superposition of temperature rises due to both active layers. The number of thermal masks required for each layer is linearly proportional to the number of active layers. Thus, two thermal masks for each active layer (four in total) are required for 3D IC configuration shown in Fig. 7. Likewise, two intrinsic error profiles per layer (four in total) are needed for intrinsic error computation.




Temperature Profile at the layer 1 ($T_1$) =
Temperature rise at layer 1 due to heat from layer 1 and 2
Temperature Profile at the layer 2 ($T_2$) =
Temperature rise at layer 2 due to heat from layer 1 and 2

**FIGURE 7. A Schematic diagram of heat flow in a two-stack 3D IC.**

The thermal masks are obtained as follows. First, apply point heat source to the center of the first layer and then thermal impulse responses are obtained at both layers. Similarly, another point heat source is applied to the center of the second layer. The rest of the procedure is the same. Figure 8 shows four thermal masks for the two-stack 3D IC.

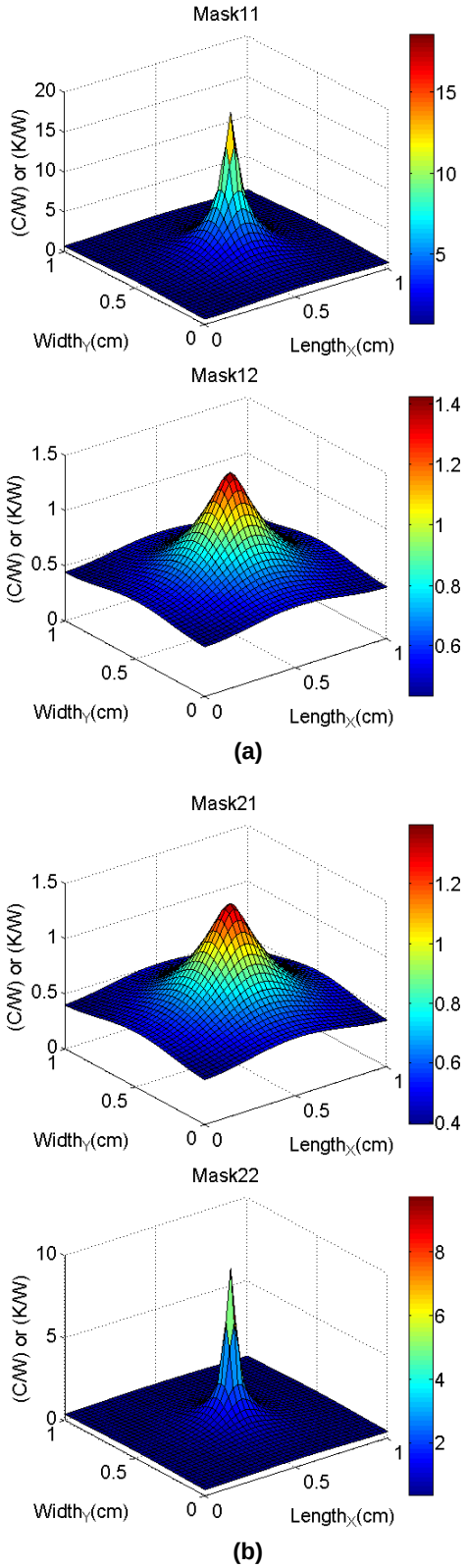



**FIGURE 8. Four thermal masks: (a) two thermal masks for the first layer and (b) two thermal masks for the second**

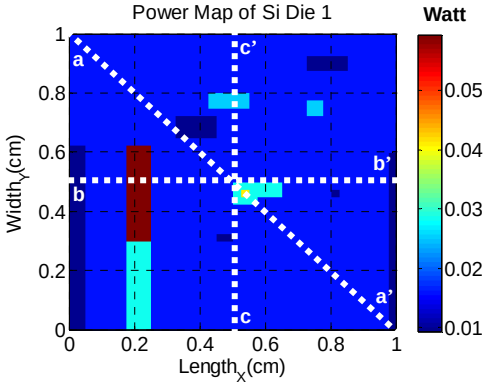
**layer ("$Mask_{AB}$" denotes thermal mask obtained at layer A with a point heat source at layer B).**

Once the multiple thermal masks and intrinsic error profiles are obtained, the rest of the procedure is the same as the PB method for 2D ICs [16]. As shown in Fig. 7, the temperature profile of one layer is obtained by sum of temperature rise due to both active layers. For example, temperature profiles of active layer 1 ($T_1$) and layer 2 ($T_2$) are given by

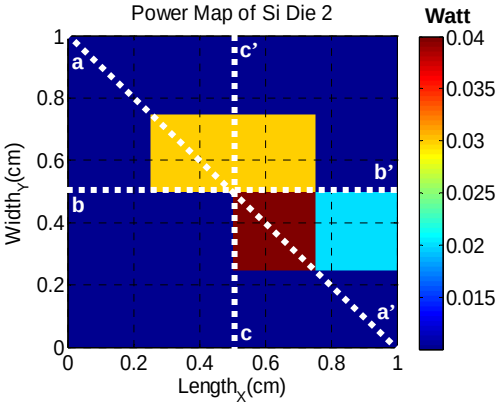
$$\begin{aligned} T_1 &= Mask_{11} * P_1 + Mask_{12} * P_2 \\ T_2 &= Mask_{21} * P_1 + Mask_{22} * P_2 \end{aligned} \quad (2)$$

where $P_1$ and $P_2$ represent the power maps of layers 1 and 2, respectively .

## RESULTS AND DISCUSSION



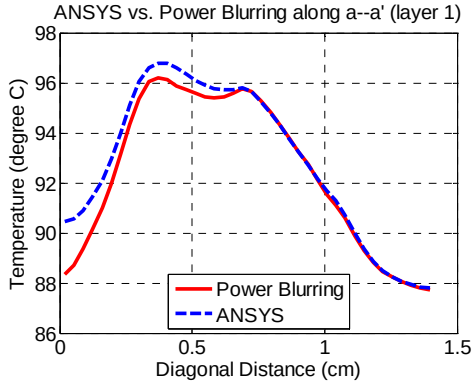

(a)

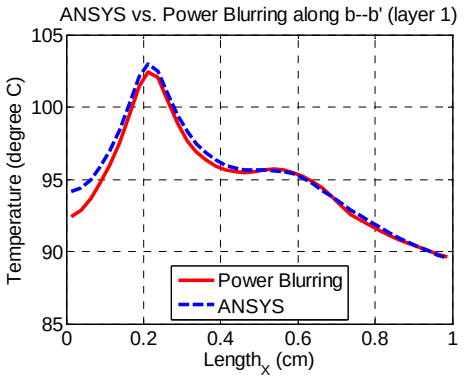


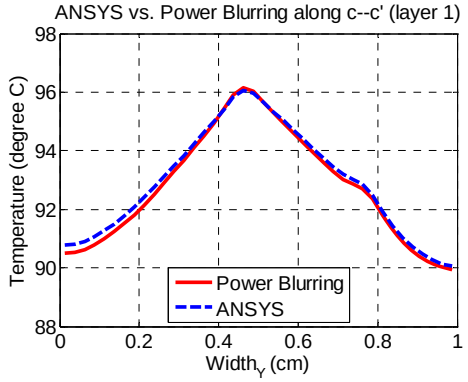

(b)

**FIGURE 9. Power map of Si die 1 (a) and Si die 2 (b)**

Figure 9 shows power maps of each active layer used for case study. Thermal profiles of each layer are obtained according to Equation (2). The PB method for 3D ICs has been validated against commercial finite element analysis tool, ANSYS. Figure 10 and 11 show our simulation results along with ANSYS simulation results for comparison. As can be seen, the proposed method yields accurate thermal profiles with maximum error less than 2% with respect to ANSYS simulation results and reduces computation time from 40.4 seconds to 0.7 second. The difference in computation time is much more when finer mesh is used as finite element is inherently volume simulation while power blurring is a surface technique [add ref.].



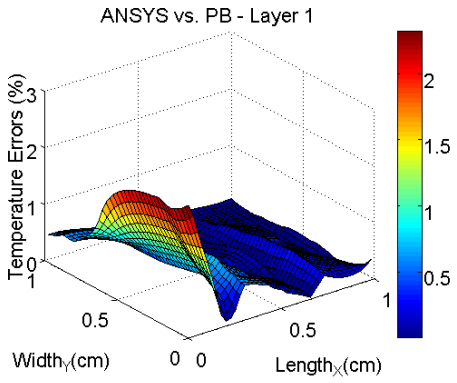



**Figure 10. Thermal profiles of layer 1 along various paths defined in Fig. 9, and overall relative error with respect to ANSYS simulation result.**

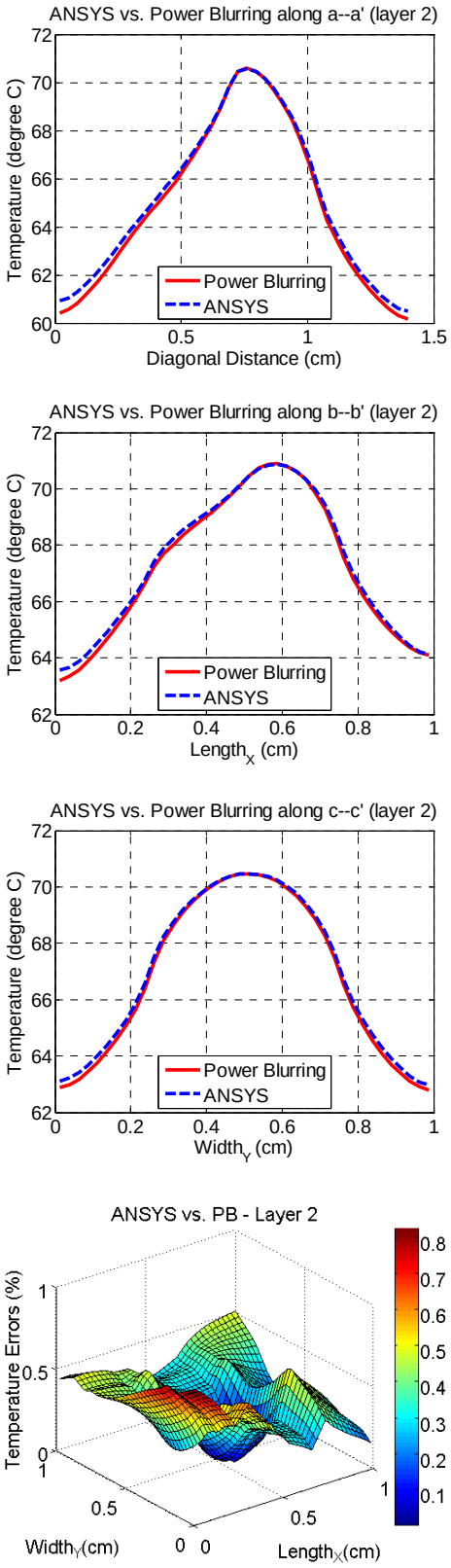



**Figure 11. Thermal profiles of layer 2 along various paths defined in Fig. 9, and overall relative error with respect to ANSYS simulation result.**

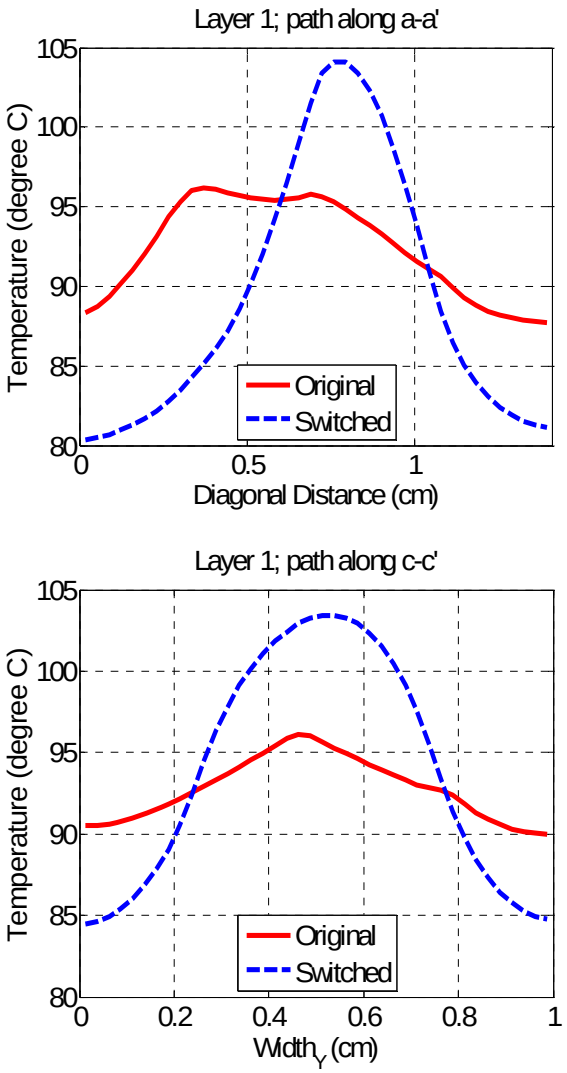



**FIGURE 12. Thermal profiles of layer 1 along path a-a' and c-c' with switched power maps.**

To explore the thermal impact of the 3D geometry, thermal profiles with switched power maps are compared with original configuration. The temperature difference is more prominent on the layer 1, and the comparison is shown in Fig. 12. The overall maximum temperature difference is as much as 15°C. This is due to the existence of bonding material between the Si dies, which has relatively low thermal conductivity. For 3D ICs, not only cell placement but also the order of stacked dies needs to be taken into account for thermal optimization.

## CONCLUSION

2D power blurring method was extended to accommodate 3D chip thermal analysis. It requires multiple spatial impulse responses (thermal masks or Green's functions) corresponding to each active layer, which can be obtained by using FEA tools

such as ANSYS or through measurement. The thermal mask is convoluted with a power map to generate a temperature profile. For 3D chips, the superposition principle is applied. When the chip geometry is simple, typically 1D heat flow, the thermal mask can be found analytically. However for realistic chip geometries, where heat spreading is important, two ANSYS simulations per layer (one for a point heat source in the center and the other for uniform heat distribution) are enough to fully characterize the 3D chip. The temperature resulting from any arbitrary power dissipation in each layer of the 3D chip can be computed quickly using convolution. For 3D ICs, not only cell placement but also the order of stacked dies needs to be taken into account for thermal optimization.

## ACKNOWLEDGMENTS

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