

Nanoscale Devices for Solid State Refrigeration and Power Generation

Ali Shakouri

Jack Baskin School of Engineering,
UC Santa Cruz, Santa Cruz CA, 95064
ali@soe.ucsc.edu

Abstract

A brief review of various techniques to engineer nanoscale thermal and electrical properties of materials is given. The main emphasis is on various energy conversion mechanisms, particularly, thermo electric refrigeration and power generation. Recent experimental and theoretical results on superlattice and quantum dot thermoelectrics and solid-state and vacuum thermionic thin film devices are reviewed. We also present an overview of the research activities at the multi university Thermionic Energy Conversion Center on the design of solid-state and vacuum devices that could convert heat into electricity with hot side temperatures ranging from 300 to 650C and with high conversion efficiency.

Keywords

Nanotechnology, Thermoelectrics, Thermionics, Energy Conversion, Quantum Dots, Superlattices, Micro Refrigeration

1. Introduction

Nanotechnology is promising to be a disruptive technology that can solve problems in industries as disparate as telecommunication, biotechnology, microelectronics and energy. It can be broadly defined as “working at atomic, molecular and supra molecular levels, in the length scale of approximately 1-100nm range, in order to understand and create materials, devices and systems with fundamentally new properties and functions due to their small structure”^[1]. Usefulness of miniaturization has been known for many years in various fields such as in microelectronics and more recently in micro electro mechanical systems (MEMS). Systems with less space, material, energy and usually faster performance can be realized. In addition, in the nanometer domain there are new phenomena and properties which are unique. Two such effects are quantum phenomena and enhanced surface effects^[2,3]. An important requirement of nanotechnology is reproducible manufacturing. This can be achieved using top-down and bottom-up approaches. In the top-down approach, techniques such as photolithography are used to fabricate millions of transistors with sub micron feature sizes. Based on the 2003 International Technology Roadmap for Semiconductors (ITRS), the feature size will be reduced from current value of 0.1-0.13 μm down to 0.045 μm (=45nm) by 2010^[4]. Several manufacturers are developing deep UV lithography systems, low-k dielectrics, copper interconnects, etc. to meet these challenges. In order to produce sub 50nm structures, bottom up approaches based on self assembly are also being investigated^[5]. This is similar to the formation of molecules, polymers and crystals in nature. By modifying the local environment of atoms and molecules, artificial materials are synthesized. This technique has been very successful in

chemistry and in material science producing compounds with improved mechanical, electrical, optical, thermal or chemical properties. Now the emphasis is to produce directly nanoscale devices and systems that could be used e.g. in computation or communication applications.

2. Nanoscale electronic and thermal properties

Quantum mechanical properties of electrons have been used to engineer electronic device characteristics for more than 30 years. Confinement of electrons in sub 10-20nm thick layers (quantum wells) limits the range of available energy states to some discrete values. This energy quantization significantly modifies, for example, the interaction of electrons and photons which is the basis of many optoelectronic devices such as quantum well lasers. Changing the quantum well thickness and strain, changes the separation between different energy levels. This can change the color and polarization of light emitted by the laser. Confinement of electrons reduces the threshold current necessary to turn on the laser. In addition, high speed modulation and temperature sensitivity of the semiconductor lasers can be improved. In the case of electronic devices, modulation doping and electron confinement in a thin layer (also called two-dimensional electron gas, 2DEG) has permitted large increases in the electron mobility due to the separation between ionized donors and free electrons by nanometer thin barriers. This is the basis for high electron mobility transistors (HEMTs). In another beautiful application of quantum mechanics, superlattices which are made of a periodic arrangement of nanometer thick semiconductors have been used to make long wavelength lasers and THz sources. In this case, in addition to the bulk crystal periodicity, there is a second artificial periodicity by depositing alternate layers of two materials. This periodic potential affects significantly the wave properties of electrons and subsequently their energy and motion. Current research in nanoscale electronic devices focuses on carbon nanotubes, quantum wires and quantum dots, where the additional confinement of electrons is used to make compact high performance components. Single electron and single molecular devices are considered to be the ultimate miniaturization. More recently, the use of electron spin to encode information has added another degree of freedom to design devices. Spintronics is an emerging field where quantum mechanical superposition of electron spin states is used as a mean to process information much faster using quantum computing algorithms^[6].

Enhanced surface effects in nanoscale material have been used extensively in chemical synthesis and catalysis. With the advent of MEMS in 1980's it has been realized that most of our intuition for the operation of mechanical devices in macro scale fails in micro scale due to the increased surface effects.

Bulk forces, such as inertia, are not a limiting factor anymore. Instead surface forces such as Van der Waals are more important. Some of the macroscopic notions such as friction need to be revisited as well.

In the area of thermal transport, research in nanoscale properties is relatively more recent. The main reason may be the difficulty to measure and model micro and nanoscale thermal properties accurately [7,8,9]. Small thermocouples at the tip of atomic force microscopes (also called scanning thermal microscopy, SThM) have been successfully used to measure temperature with <100nm resolution [10]. Femtosecond laser technology has permitted measurement of heat transfer and acoustic velocities in thin film sub micron structures [11,12]. Thermoreflectance imaging using visible wavelengths has been used to measure surface temperature of integrated circuit (IC) chips with submicron spatial resolution and 50-100mK temperature resolution [13,14,15,16]. Recently this technique has been extended to backside through the substrate thermal imaging using near infrared (1.3 μ m) thermoreflectance [17].

In analyzing random thermal vibration of atoms in a solid, one typically uses eigenmodes of the vibrations, which are called phonons. Depending on the type of these vibrations, we can have longitudinal and transverse modes. Acoustic and optical phonons refer to the case where neighboring atoms oscillate in phase or out of phase, respectively. In the latter case, an atomic dipole is formed that could interact with photons, thus the name optical phonon. When one area of the sample is hot, interaction between neighboring atoms causes the random vibrations to propagate in the material. Heat conduction is usually described by the bulk parameter of thermal conductivity which is of great importance in electronic thermal management. It has been recognized for sometime that at microscale or at very short times, the parabolic heat conduction equation that assumes instantaneous effect of boundaries everywhere in the domain is not a good approximation. Hyperbolic heat equation and the more general phonon Boltzmann transport equation have been investigated. Additional parameters such as heat drag are necessary in order to take into account finite propagation velocity of vibrations and non-equilibrium effects [18]. Ballistic electron and phonon transport without any scattering over nanometer distances has a strong impact on heat generation in submicron electronic devices [19,20]. Furthermore, at interface between two solids, depending on the coupling between atoms, there could be an extra thermal boundary resistance (this is also called Kapitza resistance which was introduced in 1950's for liquid helium). There is no unified theory to describe heat conduction across boundaries and in nanometer thick layers [21,22]. Sometimes, phonons are treated as particles and their transport across an interface is described using specular or diffuse reflectance model. This depends on the roughness and scattering at the interface. In some other applications, heat and phonons are treated as waves and their transport across an interface or a multi layer is described by the acoustic mismatch model. Various experimental results have been explained using these two theories [9,23,24]. Since thermal conductivity is an average bulk effect involving many lattice vibrations (phonons

modes), it is hard to differentiate between various contributions and gain an accurate understanding of heat transport in nanometer structures. In the case of electron transport, interaction of charged carriers with electric and magnetic fields and effects such as Hall voltage and Shubnikov-de Haas oscillations are used to measure electron effective mass, mobility, number of free carriers and differentiate between electrons from different bands in the solid. This has been extremely useful to study electron transport in nanometer thick layers. Lack of similar complementary measurements in the case of phonon transport and the added difficulty due to the fact that phonons are "quasi" particles (eigenmodes) that could be annihilated or created, makes detailed analysis very difficult.

3. Nanoscale thermoelectric properties

Conventional thermoelectric (TE) coolers are based on the Peltier effect at the metal/semiconductor junction [25,26,27]. The Peltier effect is the reverse of the thermocouple effect. When the current flows from material (a) into material (b) and then back to material (a), it heats the first junction and cools the second one (or vice versa). Thus, heat is transferred from one junction to the other one. This is due to the fact that electron gas carries not only a charge but also some average transport (kinetic) energy. When electrons flow from a material in which they have an average transport energy that is lower than the Fermi energy, to another material in which their average transport energy is higher, they absorb thermal energy from the lattice, and this will cool the junction between the two materials. One could think of electron gas as expanding in the energy space as they enter the second material and this is the main reason for refrigeration. This process is reversible, if the direction of current is changed, energy is released to the lattice and there will be heating at the junction. When electrons move under an external electric field, their "average kinetic energy with respect to the Fermi level" is the exact definition of the Peltier coefficient. Lord Kelvin showed in 1851 [26] that the Peltier coefficient is the Seebeck coefficient (used to describe thermocouples) times the absolute temperature. One should note that Fermi level and temperature are critically important in the statistical mechanical description of electron gas that is in equilibrium with a reservoir exchanging both energy and particles. If an electron whose energy is equal to Fermi level is exchanged with the reservoir, this does not require an exchange of energy with that reservoir, however exchange of electrons with energies different from the Fermi level will require an exchange of energy.

The efficiency of a thermoelectric energy converter device is described by a dimensionless parameter ZT . It is given by $ZT = \sigma S^2 T / \beta$, where T is the absolute temperature, σ and β are the electrical and thermal conductivities of the material, respectively, and S is the Seebeck coefficient. A Good thermoelectric material should have high electrical conductivity to minimize Joule heating as current flows in the material, low thermal conductivity to prevent thermal shorting between hot and cold junctions and a high Seebeck coefficient for maximum conversion of heat to electrical power or electrical power to cooling. The thermoelectric

material most often used in today's Peltier coolers is an alloy of Bismuth Telluride (Bi_2Te_3) with $ZT \sim 1$. Their maximum cooling around room temperature is about 70°C , however the cooling power density is low, on the order of $5\text{-}10\text{ W/cm}^2$. Conventional thermoelectric modules have a low efficiency on the order of $6\text{-}8\%$ of Carnot value compared to $40\text{-}50\%$ for compressor based refrigerators. The amount of heat generation at the hot side for $20\text{-}30^\circ\text{C}$ cooling could be double the amount of heat removed from the cold side [26,28,29]. The micro and nanoscale electronic devices can generate $100\text{-}1000\text{ W/cm}^2$ heating, which is far beyond the capability of current TE modules. The maximum cooling power density of a TE module is inversely proportional to the length of its elements (distance between hot and cold junctions) [25,26]. However it is a challenge to manufacture thermoelectric elements with lengths smaller than $200\text{-}300$ microns. Non-ideal effects such as metal-semiconductor contact resistance inside the TE module and the finite thermal resistance of the heat sink start to dominate as the TE module is miniaturized. Some ultra-thin TE modules are available commercially [30]. They can reach cooling power densities on the order of $50\text{-}100\text{ W/cm}^2$.

Electron confinement and energy quantization in nanoscale materials change significantly the density of electronic states and various scattering mechanisms. This, in turn, can modify the thermoelectric properties of the material. This approach was suggested first for quantum wells in a pioneering work by Dresselhaus and co-workers [31,32]. A single quantum well, however, cannot be used to build useful devices because the film is too thin (typically less than a few hundreds angstroms). In-plane electron transport in a multilayer structure was therefore used in the proof-of-concept experiments [33]. For multilayer structures such as superlattices, three questions were raised on the effectiveness of the quantum confinement approach [34,35,36]. One is that electrons will tunnel through the barrier layer when the barriers are very thin. The second argument is that the barrier does not contribute to the thermoelectric transport but does contribute to the reverse heat conduction. And finally, there is also concern of interface scattering of electrons in narrow wells. A possible approach for improving performance is to use the quantum confinement effects inside both the quantum well and the barrier layer, and to have electrons in different carrier pockets in momentum space confined in different regions [37,38]. Additionally, the thermal conductivity of very thin superlattices can be reduced due to interface scattering [39]. A natural extension of quantum wells and superlattices is to quantum wires [40,41]. Theoretical studies predict a large enhancement of ZT inside quantum wires due to additional electron confinement. Experimentally, different quantum wire deposition methods have been explored [42,43,44,45,46]. However, so far, there are no experimental results on significantly enhanced thermoelectric properties of quantum wires. This is due to the difficulty to contact individual wires and make accurate thermo electric measurements. In the case of nanowire arrays, the whole structure has been embedded in an alumina template or in a polymer. Difficulty to ensure good electrical contact to all wires in an array and quantum wire size variations has impeded quantitative characterization

of low dimensional properties. Recently, Harman's group has shown that quantum-dot superlattices have a significantly higher ZT than their corresponding bulk materials reaching values on the order of 2 at room temperature [47,48]. At this stage, no models exist to quantitatively explain the observed increase in ZT . Due to the sensitivity of quantum dot energy levels to its size and the large size variations in a $100\mu\text{m}$ thick material made from thousands of quantum dot layers, it is difficult to imagine enhancement in thermoelectric power factor ($S^2\sigma$) due to sharp features in individual quantum dot density-of-states. Increased phonon scattering (reduced thermal conductivity) and possibly electron energy filtering could be the cause of enhanced ZT values.

Since early 1990's there have been a lot work in the area of bulk thermoelectric materials such as skutterudites, clathrates, half-heusler materials, etc. [49,50]. Even though thin film deposition techniques are not used, the main idea is to engineer nanoscale atomic properties to have a material with good electrical conductivity and low thermal conductivity. This is also called electron crystal phonon glass material following the pioneering work of Slack [26,51]. For example, the concept of a heavy rattler atom in a cage of covalently bonded crystal is used to scatter dominant phonon modes in heat conduction but ensure good electrical conductivity for electrons. High ZT values on the order of $1.5\text{-}2$ at high temperatures $>500\text{K}$ have been achieved [49]. Performance of thermoelectric coolers for cryogenic applications has also been improved. $ZT \sim 0.8$ at 225K is obtained for CsBi_4Te_6 material [52].

4. Recent advances in micro scale thermoelectric refrigerators

During the last couple of years, there have been significant advances in thin film thermoelectric coolers demonstrated at various research laboratories. Venkatasubramanian et al. at Research Triangle Institute have demonstrated $3\text{-}5$ micron thick, 100 micron diameter BiTe/PbTe superlattice coolers with maximum cooling of $\sim 30^\circ\text{C}$ and cooling power density exceeding 500 W/cm^2 (this is an estimated value and not directly measured) [53]. These values have been achieved with the use of electron transmitting, phonon blocking superlattices. Ultra low metal/semiconductor contact resistance on the order of $10^{-8}\ \Omega\text{cm}^2$ has been obtained and mounting on $10\mu\text{m}$ thick metal on top of silicon substrate was used to minimize thermal resistance at the hot junction of the thin film. A variable thickness transient Harman technique was used to estimate the thermoelectric figure-of-merit. ZT values on the order of 2.4 for p-type devices have been obtained at room temperature. Böttner et al. at Fraunhofer Institute have been working on monolithic integration of conventional BiTe and BiSbTe bulk material on silicon substrate [54]. They have been able to deposit $20\text{-}micron$ thick legs using sputtering and integrated circuit fabrication techniques to produce coolers on large scale (on $4''$ silicon wafers). They have demonstrated maximum cooling of $\sim 12^\circ\text{C}$ with a 3 p- and n-leg for a current of $\sim 1\text{A}$. The estimated cooling power density is $\sim 100\text{ W/cm}^2$. Uttam Ghoshal et al. demonstrated improved thermoelectric performance with bulk p-type $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3$ and n-type

$\text{Bi}_2\text{Te}_{2.9}\text{Se}_{0.1}$ material system with the use of sharp nanometer size point contacts at the cathode electrode. The mechanism for improvement is not yet known but a cooling enhancement by about a factor of two at low current values compared to the bulk modules has been achieved [55]. Snyder, Fleurial et al. at NASA Jet Propulsion Laboratory have used an electrochemical deposition technique to form thousands of n- and p-type $(\text{Bi,Sb})_2\text{Te}_3$ legs with a diameter of $60\mu\text{m}$ and with a thickness of $20\mu\text{m}$. Maximum cooling on the order of 2C has been measured [56].

5. Thermionic emission cooling and power generation

Thermionic energy conversion is based on the idea that a high work function cathode in contact with a heat source will emit electrons [57]. These electrons are absorbed by a cold, low work function anode separated by a vacuum gap, and they can flow back to the cathode through an external load where they do useful work. Practical vacuum thermionic generators are limited by the work function of available metals or other materials that are used for cathodes. Another important limitation is the space charge effect. The presence of charged electrons in the space between the cathode and anode will create an extra potential barrier between the cathode and anode, which reduces the thermionic current. The materials currently used for cathodes have work functions $> 0.7\text{ eV}$, which limits the generator applications to high temperatures $>500\text{K}$. Mahan [58] proposed these vacuum diodes for thermionic refrigeration. Basically, the same vacuum diodes which are used for generators will work as a cooler on the cathode side and a heat pump on the anode side under an applied bias. Mahan predicted efficiencies of over 80% of the Carnot value, but still these refrigerators only work at high temperatures ($>500\text{K}$). There has been recent research to make efficient thermionic refrigerators at room temperature with the use of nanometer thick vacuum gaps [59]. This is sometimes called thermotunneling. This idea is based on the fact that electron tunneling increases exponentially as a function of barrier thickness. Use of $<5\text{-}10\text{nm}$ barriers will allow conventional metal electrodes to achieve appreciable emission currents (100's A/cm^2) and cooling power densities (100's W/cm^2) at room temperature. There have been detailed theoretical studies and some preliminary experimental results [59], however no substantial cooling has been achieved. The main difficulty is to produce uniform nanometer size vacuum gaps over large areas and to maintain the gap as temperature gradient, thermal expansion and mechanical stress develop. In another approach, sometimes called inverse Nottingham effect, resonant tunneling at appropriately engineered cathode band structure has been proposed to enhance vacuum emission currents [60,61]. Use of enhanced field emission at nanostructured surfaces, such as carbon nanotubes or sharp tips, has also been investigated theoretically and experimentally [62,63]. While significantly increased vacuum currents have been obtained [64,65], there are no experimental results on refrigeration or energy conversion near room temperature. It is important to note that the "selective" emission of hot electrons (energies higher than the Fermi level) compared to cold electrons (energies lower than the Fermi level) is necessary in order to achieve refrigeration or

thermal to electric energy conversion. Since at room temperature the energy distribution of electrons inside Fermi window is on the order of $25\text{-}50\text{meV}$, a precise engineering of tunneling is necessary to achieve appreciable energy conversion. Recently, Koeck et al. have demonstrated vacuum power generation with nanostructured nitrogen-doped diamond emitter separated by $\sim 80\mu\text{m}$ gap from collector. At a cathode temperature of 825C , substantially below conventional vacuum thermionic modules, 120mV thermo voltage was generated [66,67].

Shakouri and Bowers first proposed to use thermionic emission in heterostructure barriers for cooling applications at room temperature [68,69]. This is called heterostructure integrated thermionic (HIT) coolers. The advantage of semiconductor barriers is that small barrier heights on the order of $0.1\text{-}0.2\text{eV}$ can be easily and accurately fabricated. The disadvantage is that cathode and anode are not separated in vacuum. Cooling at the cathode has to fight the parasitic heat from anode through semiconductor barrier layer. Initial calculations based on nonlinear transport regime showed high cooling power densities exceeding 100's W/cm^2 could be achieved [69, 70]. In this design, it is necessary to use several microns thick barrier and optimum barrier height at the cathode on the order of thermal energy of electrons, $k_{\text{B}}T$, where k_{B} is the Planck's constant. Large barrier height at the anode to reduce reverse current is also needed. A few single barrier InGaAs/InGaAsP/InGaAs thin film devices lattice matched to InP substrate were fabricated and characterized [71]. The InGaAsP barrier ($\lambda_{\text{gap}}\sim 1.3\mu\text{m}$) was one micron thick and $\sim 100\text{meV}$ high. Even though cooling by 1C and cooling power density exceeding 50W/cm^2 were achieved [71,72], it was not possible to increase the bias substantially and benefit fully from large thermionic emission cooling. This is due to the non-ideal metal-semiconductor contact resistance and Joule heating in the substrate. The single barrier HIT device in nonlinear transport regime was not anticipated to have an improved conversion efficiency and the main emphasis was on temperature stabilization of optoelectronic devices with monolithic structures [73,74]. In 1998 Mahan and Woods proposed to use thermionic emission in multi layer structures in linear transport regime with an estimated factor of two increase in the figure-of-merit ZT [75]. Based on this idea, a few structures were synthesized by Kim et al., however due to poor material quality no improvement was reported [76]. Later calculations by Radtke et al. [77] showed that in the linear transport regime the thermoelectric power factor in multi layer thermionic devices is smaller than that of thermoelectric one and thus the main advantage of superlattices is in the reduction of phonon thermal conductivity. Mahan and Vining in a subsequent publication reached the same conclusion [78]. This analysis was also based on linearized ballistic transport over symmetric barriers.

In contrast to the previous publications Shakouri et al. in 1999 proposed that tall barrier, highly degenerate superlattice structures can achieve thermoelectric power factors an order of magnitude higher than the bulk values [79]. No assumption about ballistic transport was made and the improvement was solely due to the filtering of hot electrons in a highly degenerate sample. Recently the theoretical analysis of

electric and thermoelectric transport perpendicular to superlattice direction has been revisited^[80,81]. It is shown that highly degenerate semiconductors and metallic-based superlattices in the quasi-linear transport regime have the potential to achieve thermoelectric power factors significantly larger than bulk values. Assuming a lattice contribution to thermal conductivity on the order of 1W/mK, ZT values exceeding 5-6 are predicted. The key requirement is non-conservation of lateral momentum during thermionic emission process. This will allow much larger number of hot electrons to participate in the conduction process. This could be achieved using non-planar barriers or embedded quantum dot structures^[80,81]. It is important to note that the role of quantum dots in this case is quite different from low dimensional thermoelectrics. Discrete energy states are not directly used. Quantum dots acts as three dimensional scattering centers and energy filters for electrons moving in the material.

In May 2003 a new multi university research initiative on thermionic energy conversion started with funding from Office of Naval Research^[82]. Thermionic Energy Conversion center is composed of research groups at Universities of California at Santa Cruz, Berkeley and Santa Barbara, Harvard, Massachusetts Institute of Technology, Purdue and North Carolina State University. The goal is to develop direct thermal to electric energy conversion systems that could operate at hot side temperature of 300-650C with high efficiencies (>15-20%) and with high power densities (> 1W/cm²). This will provide an attractive compact alternative to internal combustion engines for many applications in the watt-mega watt range. This will also expand the possibilities for waste heat recovery applications. Thermionic Energy Conversion (TEC) center goal is to design, fabricate and characterize direct energy conversion systems that meet the above requirements. The core of the solution is an integrated approach to engineer electrical, thermal and optical properties of nanostructured materials and devices in order to fabricate more efficient solid-state and vacuum-based thermionic energy conversion components and systems. Novel metallic based superlattices with embedded quantum dots are synthesized by molecular beam epitaxy and by pulsed laser deposition systems. Nanostructured carbon, highly oriented diamond and low electron affinity nitride vacuum emitters are also grown. Both bulk and nanoscale electrical and thermal properties are measured using techniques such as ballistic electron emission microscopy, scanning thermal microscopy, X-ray photoelectron emission spectroscopy, etc. The main emphasis is to understand the local electronic, thermoelectric and heat transport properties. Finally, various components will be integrated and packaged for systems demonstration. While the main emphasis is on energy generation at higher temperatures, many of the concepts and techniques developed at the center could also be used to improve the room temperature solid-state refrigerator devices.

6. Heterostructure Integrated Thin Film Coolers

One attractive solution for microscale temperature control is to monolithically integrate thin film coolers with active electronic devices inside integrated circuits. In a collaboration

between UCSC, UCSB, Berkeley, Harvard and HRL Laboratories, Shakouri, Bowers et al. have been working on the use of thermionic emission in heterostructures in order to improve the cooling performance of conventional semiconductors used in microelectronics and optoelectronics. Several metal organic chemical vapor deposition (MOCVD) grown (InGaAsP/InP^[83] and InGaAs/InP^[84]), and molecular beam epitaxy (MBE) grown (InGaAs/InAlAs^[85], InGaAsSb/InGaAs^[86], SiGe/Si^[87], and SiGeC/Si^[88]) heterostructure integrated thermionic (HIT) microcoolers have been fabricated and characterized. These structures were lattice matched to InP or silicon substrates to ease the monolithic integration. Different superlattice periods (5-30nm), dopings (1×10^{15} - 7×10^{19} cm⁻³) and thicknesses (1-7 μ m) were analyzed. Various device ranging in size from 100 μ m² to 40,000 μ m² were fabricated using standard thin film processing technology (photolithography, wet and dry etching and metallization). Both n- and p-type micro refrigerators were demonstrated. Cooling by 1C at room temperature and by 2.5C at 80C ambient temperature for InP-based HIT superlattice coolers was measured. Si-based micro refrigerators had a higher cooling on the order of 4.5C at room temperature and 12C at 200C ambient temperature. In the single leg geometry, a gold or aluminum metal contact was used to send current to the cold side of the device. The Joule heating and heat conduction in this metal layer had a strong impact on the overall cooler performance. Electrical contact on the backside of silicon or indium phosphide substrate, or on the front surface far away from the device, was used as the second electrode. Thus, three dimensional heat and current spreading in the substrate helped localized cooling of the device. We observed that due to non-ideal effects (Joule heating in the substrate, at metal-semiconductor junctions and in the metal contact layer), there is an optimum device size on the order of 50-70 micron in diameter that achieved maximum cooling^[72,89,90]. This is due to the fact that various parameters scale differently with the device size. For example the 3D substrate thermal and electrical resistances scale as the square root of the device area, while Joule heating due to metal-semiconductor contact resistance scales directly proportional to it^[89,90,91]. Cooling temperature in these miniature refrigerators was measured using three techniques. First a small ~25-50 micron diameter type E thermocouple was placed on top of the device and a 2nd thermocouple was placed farther away on the heat sink. Even though the thermocouple had the same diameter as the refrigerator, accurate temperature measurements with ~0.01C resolution could be made. We also used integrated thin film resistor sensor on top of the micro cooler. To electrically isolate the thin film resistor, first 0.1-0.3 micron thick SiN layer was deposited on the top electrode of the micro refrigerator. The resistance versus temperature was calibrated on a variable temperature heating stage and this was used to measure cooling on top of the device. Resistor has the advantage that a heat load could also be applied directly on top of the device. Cooling power density was thus characterized and values ranging from 100-680W/cm² were measured. It is interesting to note that contrary to maximum cooling temperature results, the smallest samples (~30-40 micron in diameter) had the

largest cooling power densities [92]. This was explained using theoretical models and it is due to the fact that certain parasitic heat conduction mechanisms (e.g. through the metal contact to the cold junction) will reduce maximum cooling below ambient temperature, but, in fact, they can improve the cooling power density of the micro refrigerator. Finally, an optical technique based on thermoreflectance imaging was used to obtain temperature distribution on top of devices with sub micron spatial resolution and $<0.1\text{C}$ temperature resolution [16,17].

ZT of bulk SiGe is 4-5 times smaller than BiTe at room temperature and III-V semiconductors have a very low ZT of about 0.01-0.02 [93]. The main use of the above mentioned HIT coolers is not to achieve high efficiencies and to cool big macroscopic size chips. The key idea is to cool selectively small regions of the chip and remove hot spots locally. If a small fraction of the chip power is dissipated in localized regions, low thermoelectric efficiency is not the most important factor. It is more critical to incorporate small size refrigerators with minimum additional thermal resistances for the whole chip package.

When comparing HIT micro-coolers with bulk thermoelectric modules, there are mainly three advantages. First of all, micro-size and standard microprocessor fabrication method makes HIT refrigerators suitable for monolithic integration inside IC chips. It is possible to put the refrigerator near the device and cool the hot spot directly. The 3D geometry of the device allows heat spreading from a small hot region to the heat sink. Second, the high cooling power density is one of the main advantages as compared with commercial bulk TE refrigerators. In fact the directly measured cooling power density exceeding $680\text{W}/\text{cm}^2$ [92] is one of the highest numbers reported so far and it is similar to the best values achieved by thin film BiTe/PbTe superlattice coolers having a $ZT \sim 2.4$ [53]. Third, the transient response of the current SiGe/Si superlattice refrigerator is several orders of magnitude better than the bulk TE refrigerators. The standard commercial TE refrigerator has a response on the order of 10^3 's of seconds. The measured transient response of a typical HIT superlattice sample is on the order of $\sim 20\text{-}40\mu\text{s}$ again very similar to BiTe/PbTe superlattices [53].

According to the theoretical models, the current limitation of the superlattice coolers still lies in the contact resistance between the metal and cap/buffer layer, which is on the order of $10^{-6}\ \Omega\text{cm}^2$. Simulations predict $20\text{-}30^\circ\text{C}$ of cooling with a cooling power density exceeding several $1000\text{'s}\ \text{W}/\text{cm}^2$ is possible with the optimized SiGe superlattice structure. Direct integration of micro refrigerators with silicon IC chips is currently being investigated. Preliminary results show that two-chip wafer bonding could be used to provide localized cooling in integrated circuits without the need for monolithic integration [85,94].

Summary

An overview of recent advances in thin film thermoelectrics and solid-state and vacuum thermionic devices was given. The main emphasis was on the key physical mechanisms and nanoscale material engineering in

order to improve efficiency and maximum cooling or power generation capability.

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