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# Bias-dependent MOS transistor thermal resistance and non-uniform self-heating temperature

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**Abstract**

The relationship of the biasing condition and the self-heating effect of a multi-channel metallic oxide semiconductor field effect transistor (MOSFET) device was examined using various channel currents ranging from triode to saturation regimes. When temperature non-uniformity is generated due to transistor self-heating, the local thermal resistance is conventionally defined through the difference between the hottest local temperature and the backside temperature. It was found that the thermal resistance independence of the input power is only valid if we take into consideration the size and shape change of the heating body. We show in this paper the evolution of MOSFET self-heating through both direct thermoreflectance imaging observation and a three-dimensional analytical heat dissipation model of the device. The device thermal resistance obtained can change by a factor larger than 5 for different drain–source voltages. Even in the saturation regime, the thermal resistance of the transistor can change by 50% as a function of the bias.

(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

The rapid growth in the microelectronic industry has led to an aggressive increase in switching and further miniaturization of the device feature sizes [1, 2]. Thermal issues are more critical than ever and have become one of the key factors limiting the state-of-the-art device and integrated circuit performance and reliability. Among the various thermal issues, self-heating induced failure has been recognized as one of the major reliability issues not only on the device level but also on the circuit level, which is consequently affected by the device thermal performance. Therefore, systematic characterizations of fundamental thermal effects inside single devices are very important.

A field effect transistor (FET) is a three-terminal device, where a non-uniform electrical potential distribution is naturally created. This electrical potential field together with the current flow along the channel generates a non-uniform temperature distribution (*hot spot*), which is usually located towards the drain end for a typical metallic oxide semiconductor field effect transistor (MOSFET). This temperature rise can further cause changes in the material properties and thus cause changes in the characteristic of the device. The introduction of novel geometries and materials in modern transistors has made non-uniform self-heating effects even more pronounced [1–4].

Non-contact thermoreflectance imaging is capable of obtaining thermal images with both high spatial resolution (sub-micrometres) and temperature resolution (sub-kelvin) [5, 6]. It has recently been utilized to characterize the heating effects in metallic oxide semiconductor transistors [7]. However, the work of Burzo *et al* [8] emphasized demonstrating the applicability of the experimental system, but did not provide detailed discussions about the heating inside the transistor.

In this study, we have performed systematic thermal characterization and analyses based on an n-type depletion mode multi-channel MOSFET. The following section describes the experimental setup used to obtain the surface temperature distribution as well as the structure of the device. Experiment results and analysis are shown in section 3. In section 4, we compare the experiment result with the

 

simulation and discuss the bias-dependent thermal resistance of the transistor.

## 2. Experiment

The thermoreflectance imaging technique is based on a weak dependence of the material surface reflectivity on the local temperature [9]:

$$\Delta R = a(\Delta T) + b(\Delta T)^2 + c(\Delta T)^3 + \cdots. \tag{1}$$

Equation (1) shows the change in surface reflectivity as a function of the temperature change, where $R$ is the reflectivity, $T$ is the local temperature and $a$, $b$, $c$ are the material, the wavelength and the topographic structure dependent polynomial coefficients. Since this temperature induced change is very small (typically in the $10^{-4}$–$10^{-5}$ per degree range), the local temperature variation versus reflectivity relationship can be expressed using a linear approximation, shown as equation (2):

$$\Delta T = \frac{(R_1 - R_0)}{C_{\text{th}} \times R_0}, \tag{2}$$

where $R_0$ and $R_1$ are the surface reflectivities at ambient temperature and heating (cooling) temperature, respectively. $C_{\text{th}}$ is the first order thermoreflectance coefficient, which represents the sensitivity of the surface reflectivity to local temperature variation.

Because of the high sensitivity of the thermoreflectance coefficient to both the sample and the experimental conditions (material, illumination wavelength and sample surface topographic features), *in situ* calibration is required. We calibrated the thermoreflectance coefficient by introducing an external temperature variation. A fast thermoelectric cooling (TEC) stage was used to periodically change the global temperature of the device, and the intensity of the reflected light is monitored using a charge coupled detector (CCD). Through normalization, we obtained the thermoreflectance coefficient for the device, as $2.52\text{e}^{-4}\ \text{K}^{-1}$.

Figure 1 shows a schematic of the experimental setup. The illumination source is a high power light emitting diode (LED) emitting 455 nm wavelength light in the blue range. The emitted light was collimated and focused onto the specimen top surface through a high magnification objective (80×). The reflected light was then projected back to a detector through the same objective, but in a separate light path defined by a beam splitter.

Since the dependence of the reflectivity on the local temperature variation is very small, the lock-in technique is typically utilized when the device is cycled [5, 6]. As the hardware based lock-in is prohibitive for high spatial resolution full-field image detection, where hundreds of channels are carrying signals in parallel, we used the software based lock-in in our thermoreflectance imaging system. The details are described elsewhere [5, 7]. Reflected images from the specimen surface are detected by either a PIN diode array camera or a high frame rate intensified CCD (ICCD). The PIN array has a higher dynamic range and thermal resolution,

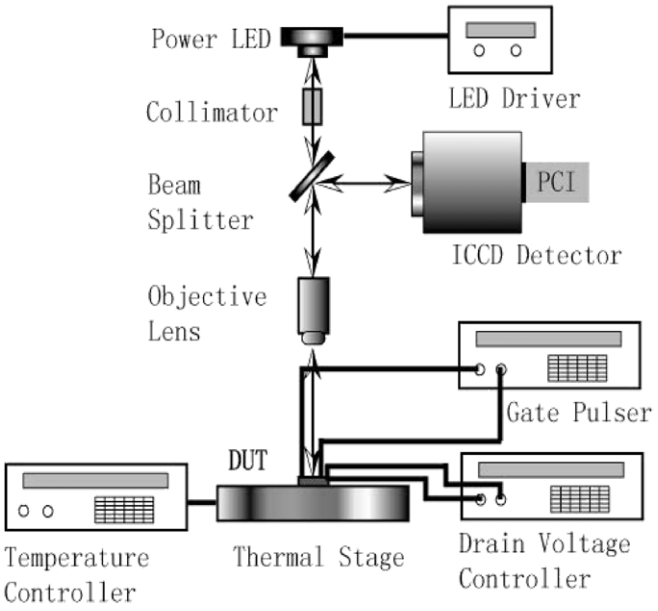


**Figure 1.** Schematic of the thermoreflectance imaging setup.

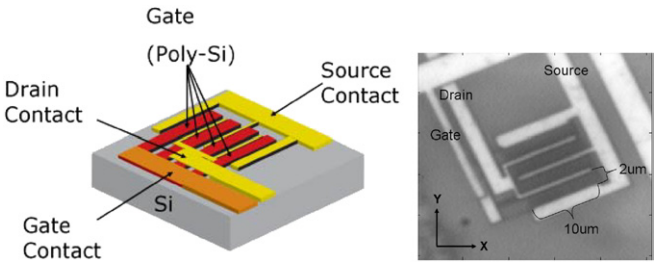


**Figure 2.** Schematic and microscopic image of the multi-channel MOSFET.

while the ICCD yields superior spatial resolution. In this experiment, ICCD was used as we were interested in the high spatial resolution temperature distribution in the device in the steady state. As for providing an efficient heat dissipation path, a thermal stage was placed immediately underneath the specimen.

During the experiment, the pulsed voltage was applied to the gate terminal, while the drain–source voltage was held constant. The CCD detector was synchronized with the gate voltage generator, so that the surface temperature variation distributions are guaranteed to be captured when the device is in the 'ON' state.

The studied MOSFET has four channels defined by alternative drain and source terminals. Poly silicon gates were formed on top of the oxide area. The structure is shown in the schematic and the microscopic image (figure 2). The purpose of the multiple gates/channels design is to increase the capacity of the operating current, as desired in telecom applications.

The sample was excited by a pulse voltage of frequency $f$ ($f = 106\,\text{Hz}$). Within a cycle $\tau$ ($\tau = 1/f$), the electrical excitation can be represented by

$$V(t) = \begin{cases} V_0 & 0 \leqslant |t| < \dfrac{\tau}{2}, \\ 0 & \dfrac{\tau}{2} < |t| \leqslant \tau. \end{cases} \tag{3}$$

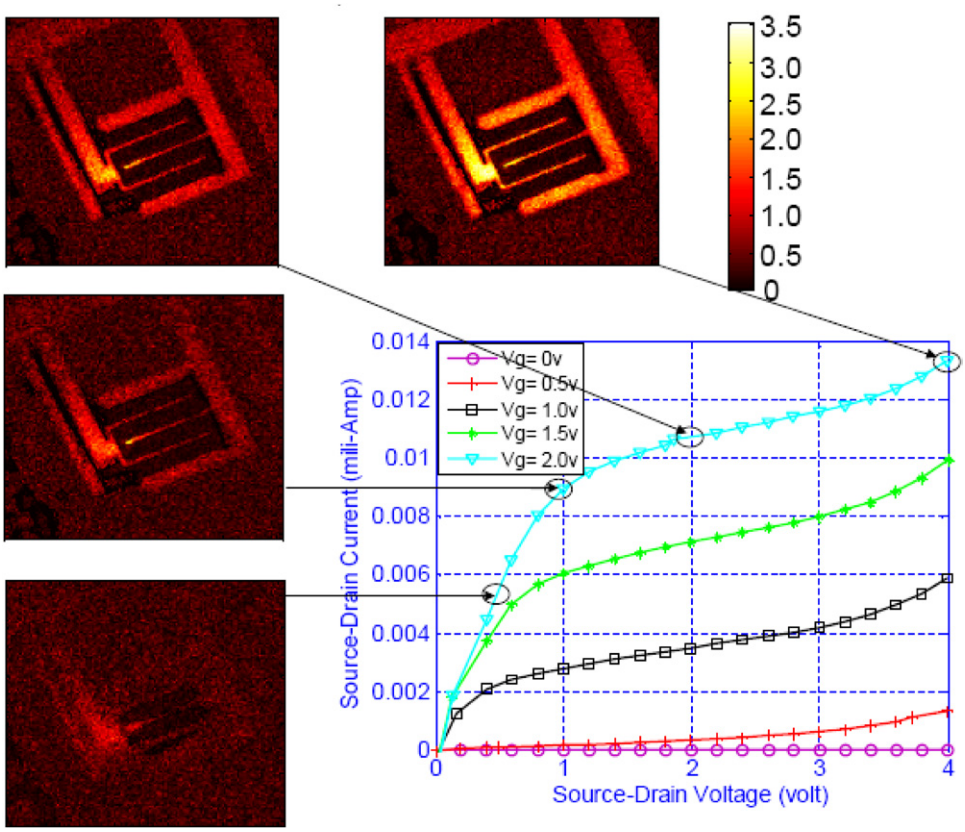


**Figure 3.** Thermoreflectance images of the multi-channel MOSFET under different biasing conditions. The temperature profile is calibrated on the metal layer.

For a transistor device, which is only a few micrometres in width and thickness, the time it requires to achieve thermal steady state is on the order of tens of microseconds. Therefore, an excitation frequency less than 10 KHz should guarantee that the device achieves thermal steady state within each excitation cycle. The choice of 106 Hz as the excitation frequency is based on the optimization of the ICCD detection sensitivity and the detection noise.

## 3. Results and discussion

The thermal resistance is conventionally defined through the difference between the hottest local temperature and the backside temperature as [10]

$$R_{\mathrm{th}} = \frac{\Delta Q}{T_{\mathrm{h}} - T_{\mathrm{b}}}, \tag{4}$$

where $\Delta Q$ represents the amount of power being dissipated, $T_{\mathrm{h}}$ is the maximum temperature at the hot spot, $T_{\mathrm{b}}$ is the backside temperature at the bottom of the substrate and $R_{\mathrm{th}}$ is the total thermal resistance in the heat flow path. Typically, for a constant backside temperature, the thermal resistance of the device is considered constant as well, if the rise in temperature due to self-heating is not high enough to cause significant changes in the local material properties [8]. In the case of an HV device, where the self-heating is relatively large, the thermal resistance change is explained purely through the change in the local material properties (mainly, substrate thermal conductivity) [3, 4].

Figure 3 shows the rise in the surface temperature of the multi-channel MOSFET under-test when different biasing conditions ($V_{\mathrm{ds}} = 0$–$4$ V, $V_{\mathrm{gate}} = 2$ V) were applied. Through the empirical power law of the temperature dependence of the thermal conductivity of Si, the change in the thermal conductivity can be estimated as

$$\Delta K_{\mathrm{th}}(T) = \alpha(T_{\mathrm{h}}^{\beta} - T_{\mathrm{b}}^{\beta}), \tag{5}$$

$$\alpha = 3110.05(\mathrm{W\,cm^{-1}K^{-1}}) \qquad [4],$$

$$\beta = -4/3 \qquad [11].$$

At the highest bias, the maximum hot-spot temperature rise (3.5 °C), only a reduction of 0.0247 $\mathrm{W\,cm^{-1}\,K^{-1}}$ is introduced to the substrate thermal conductivity. This indicates a negligible thermal resistance change due to the thermal conductivity change. Therefore, a linear dependence of the maximum hot-spot temperature rise on the input power would be expected (equation (1)) based on the conventional assumption of a constant thermal resistance.

However, plotting the maximum temperature rise versus the source-drain voltage $V_{\mathrm{d}}$ in comparison with the input power versus the source-drain voltage, we noticed a discrepancy, shown in figure 4. Before the device reaches the pinch-off, the hot-spot temperature increases in a parabolic shape rather than in a quadratic shape as the input power increases.

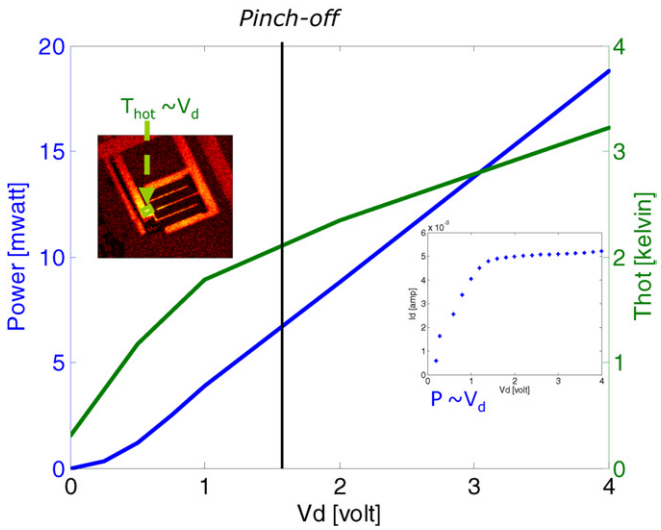


**Figure 4.** Hot-spot temperature and input power versus the source-drain voltage.

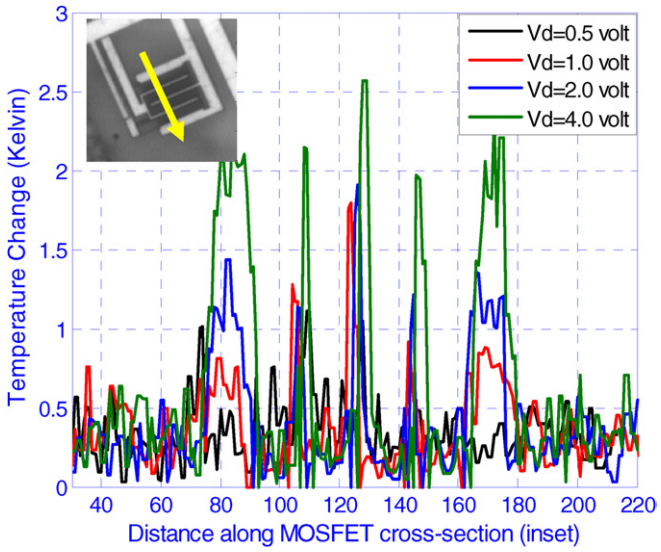


**Figure 5.** Temperature rise profiles along the cross-section.

After the device reaches the pinch-off point, although the trends of the hot-spot temperature rise increment and the input power increment are both quasi-linear, the slopes are very different. This violates Fourier's law if a constant thermal resistance in the heat flow path is assumed.

Figure 5 shows the temperature rise profiles along the drain metal cross-section. The comparison of the contour shapes of these profiles reveals an increase in the actual heating body at different biasing conditions.

Taking into consideration the variation of the heating body, we replot figure 4 using an integral of the temperature rise within the hot-spot area, rather than the single maximum temperature rise. Shown in figure 6 is the result, along with the input powers at different source-drain voltages. The full width at half heights (FWHHs) measured in the temperature histogram of each thermal image were used as a threshold value, which define the boundary of the hot-spot area. A similarity was obtained when comparing the

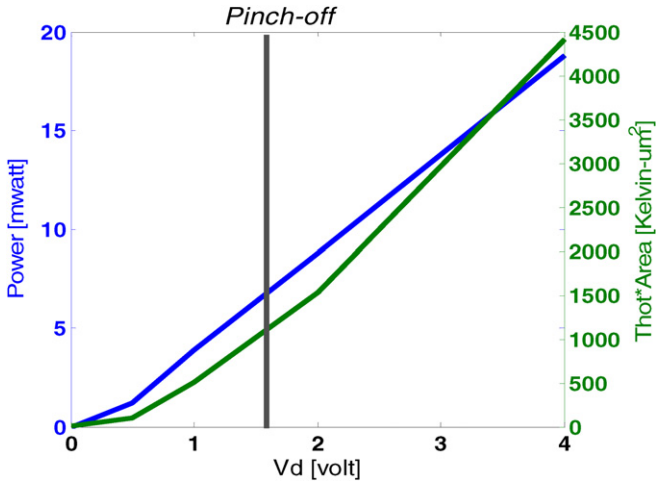


**Figure 6.** Input power and temperature integral (i.e. temperature rise multiplied by the hot-spot area (K $\mu$m$^2$) versus the source-drain voltage.

two curves in figure 6. This indicates that the discrepancy revealed in figure 4 was caused by the evolution of the actual size/shape of the hot spot at varied source-drain voltages. The remaining difference between the slopes could be due to the lack of temperature signals in the poly-gate area, where the thermoreflectance coefficient is small at the operating wavelength in this experiment.

To simulate the actual thermal resistance at different biasing conditions, we utilized a spreading thermal resistance model [12]. We approximated that the heating source has a circular contour defined by a radius $r_{\mathrm{h}}$. This heat source is placed on a silicon substrate with the radius significantly larger than that of the hot spot. A ceramic package was introduced to imitate the boundary condition at the bottom surface of the silicon substrate in a real experiment situation. Equation (6) represents the spreading thermal resistance at the hot spot:

$$R_{\mathrm{th}} = \frac{L_{\mathrm{sub}}}{A_{\mathrm{sub}}\kappa_{\mathrm{sub}}} + \frac{1}{2a\kappa_{\mathrm{sub}}\sqrt{\pi}}(1-\varepsilon)^{3/2}\Phi_C, \tag{6}$$

where

$$\Phi_C = \frac{\tanh(\lambda_C\tau) + \frac{\lambda_C}{B}}{1 + \frac{\lambda_C}{B}\tanh(\lambda_C\tau)}, \tag{7}$$

$$a = \sqrt{\frac{A_{\mathrm{h}}}{\pi}}, \qquad b = \sqrt{\frac{A_{\mathrm{sub}}}{\pi}}, \qquad \varepsilon = \frac{a}{b}, \qquad \tau = \frac{L_{\mathrm{sub}}}{b}, \tag{8}$$

$$\lambda_C = \pi + \frac{1}{\varepsilon\sqrt{\pi}}, \qquad B = \frac{hA_{\mathrm{sub}}}{\pi\kappa_{\mathrm{sub}}b}, \tag{9}$$

where $A_{\mathrm{h}}$ and $A_{\mathrm{sub}}$ are the areas of the heat source and the substrate surface, $L_{\mathrm{sub}}$ is the thickness of the silicon substrate, $\kappa_{\mathrm{sub}}$ is the thermal conductivity of the silicon substrate and $a$, $b$, $\varepsilon$ and $\lambda_C$ are dimensionless coefficients. $h$ is the heat transfer coefficient, which can be estimated as

$$h = \frac{1}{R_f A_{\mathrm{sub}}}, \tag{10}$$

where $R_f$ is the thermal resistance of the ceramic package.

**Table 1.** Geometry and material properties.

| Layer | Radius ($\mu$m) | Thickness ($\mu$m) | Thermal conductivity (W $\mu$m$^{-1}$ K$^{-1}$) |
|---|---|---|---|
| Hot spot | 2–20 | N/A | N/A |
| Silicon | 1000 | 500 | 1.3e−4 |
| Package | N/A | 1000 | 17e−6 |

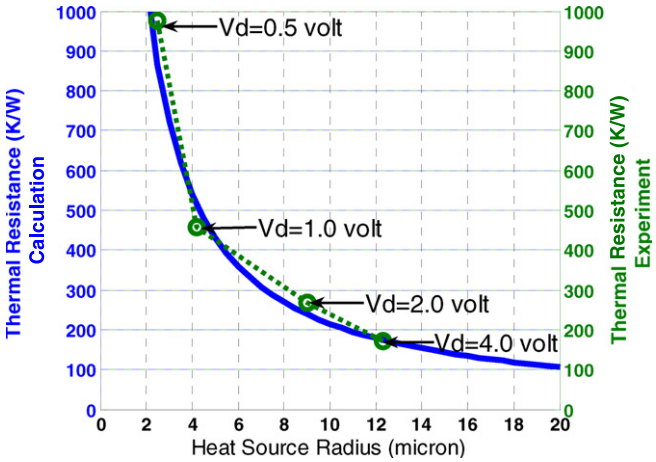


**Figure 7.** Heat source size dependence of the thermal resistance in three-dimensional heat dissipation.

Based on the geometry and material properties listed in table 1, we simulated the spreading thermal resistance at the hot spot as a function of its radius.

Shown in figure 7 is a comparison between the simulated spreading thermal resistances and the extracted thermal resistances from the measurement results. The latter were calculated using equation (1). A good fit between the simulation and the experiment was found. The calculation was done numerically using MATLAB.

## 4. Conclusions

In this paper we performed a systematic thermal characterization of a multi-channel MOSFET. We obtained high resolution thermal images using the thermoreflectance technique. Taking advantage of the full-field imaging capability of the thermoreflectance technique, we quantified the size/shape change in hot spots at various biasing conditions. We also verified the dependence of the transistor thermal resistance on biasing conditions through a comparison between the simulation and the experimental observations.

Conventionally, in the electro-thermal modelling of high power transistors, the transistor thermal resistance is extracted at small biases and short pulses and it is assumed to be a constant depending only on the geometry of the transistor [13]. We anticipate that the bias-dependent transistor thermal resistance will play an important role in the compact design of the chips and in high power circuits.

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